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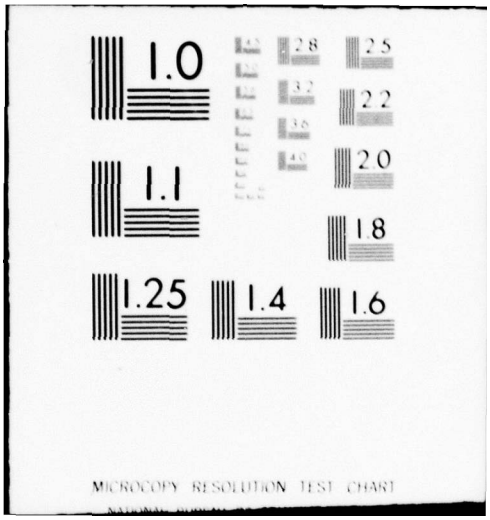
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ADVANCED TED CONCEPTS

Paul T. Greiling

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3011 Malibu Canyon Road
Malibu, CA 90265

September 1978

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Planar TELDs have been designed, fabricated, and tested. Computer models have been developed for designing and predicting the characteristics of TELDs as a function of device geometry, material parameters, and bias conditions. TELDs have been fabricated on ion-implanted LPE and VPE GaAs. Devices with as high as 24% current drop back in the I-V characteristics have been measured, and frequency dividers that divide the input signal by any integer from two through nine have been realized.

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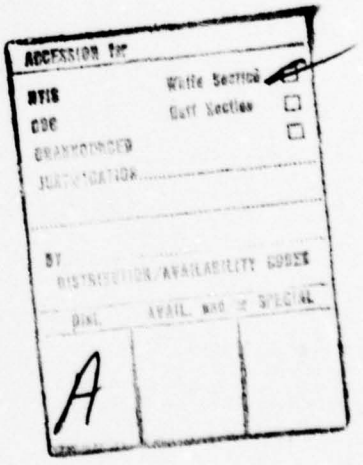

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SECTION 1

INTRODUCTION

The objectives of this exploratory development effort are to (1) design and fabricate transferred-electron logic devices (TELDs) with both Schottky-barrier and insulated pickup gates, (2) evaluate the dc and rf operating characteristics of the TELDs, and (3) correlate the measured operating characteristics with a theoretical analysis. The device structures are to be fabricated using both ion-implanted and epitaxial GaAs with silicon oxide, silicon nitride, and anodic oxide insulators.

As part of this program, planar TELDs were fabricated on ion-implanted GaAs, liquid-phase epitaxial (LPE) GaAs, and vapor phase epitaxial (VPE) GaAs. The dc current versus voltage (I-V) characteristics and the rf characteristics of the device were measured. Devices fabricated on epitaxial GaAs exhibited a current drop back of up to 24% in the dc characteristics and operated as a frequency divider dividing the input signal by an integer from two through nine.

GaAs anodic oxide has been grown with nonaqueous electrolytes. Both aqueous and nonaqueous liquid electrolytes have been incorporated; however, to be compatible with other process requirements and to minimize interface problems, nonaqueous electrolytes have been found to be the best approach.

In addition, computer models have been developed for designing TELDs. The threshold conditions were calculated as a function of device geometry, material parasitics, and bias conditions. The electric field after domain formation is computed to ensure that it is sufficient for the domain to transit from the gate to the anode. An equivalent circuit for the TELD has been used to calculate switching times as a function of device and circuit parameters.

SECTION 2

COMPUTER MODELING FOR GaAs TELDs

This section discusses the computer models developed for predicting the dc and rf performance of GaAs TELDs as a function of device geometry, material parameters, and bias conditions. Also discussed is an accurate model developed for calculating the parasitic capacitance of the device and circuit. The latter model was developed because the parasitic capacitance is an important parameter in determining the circuit speed.

Hughes has developed models for designing TELDs and predicting the switching times of the device in a circuit. To assure that a domain will nucleate and grow sufficiently to produce a large current drop back, several constraints must be satisfied. A computer model that calculates the electric field in and current density through the device before and after domain formation has been developed to design the TELD with the proper doping density and channel thickness.

For a planar TELD such as shown in Figure 1, the nl product of the device must be above the critical value[1] to ensure that a domain grows to maturity,

$$N_d l_{gA} \geq 10^{13} \quad , \tag{1}$$

since, for small N_d, the negative dielectric relaxation time is too short for a domain to form in a transit time. The energy stored in the electric field of the domain must be above the critical value,[2] which requries that

$$N_d d_o \geq 10^{12} \quad , \tag{2}$$

where d_0 is the width or thickness of the device. These constraints on domain growth determine lower bounds on the device's geometry and

doping density. The constraint imposed by Eq. 2 puts strict limits on the possibility of fabricating TELDs by ion implantation since d_o is normally between 0.3 and 0.5 μm.

An upper bound on doping density results from impact ionization occurring in the high-field region of the domain. As the doping density increases, domain growth time decreases, domain voltage increases, and the field in the domain increases. For large fields, electron-hole pairs are generated by impact ionization. Since the holes are trapped, the excess electrons will be localized at the trapped holes, thereby causing an apparent increase in the number of conduction electrons in this region. For each domain transit, the valley current is increased until domain formation becomes noncoherent. To prevent impact ionization from occurring in the domains, the doping density should be limited[3] to less than 5×10^{16} cm^{-3}. Since this restriction is based on a dc analysis for breakdown, impact ionization is time dependent, and there is a time delay in the formation of the domain, the limit based on this simple model could be exceeded to a certain extent.

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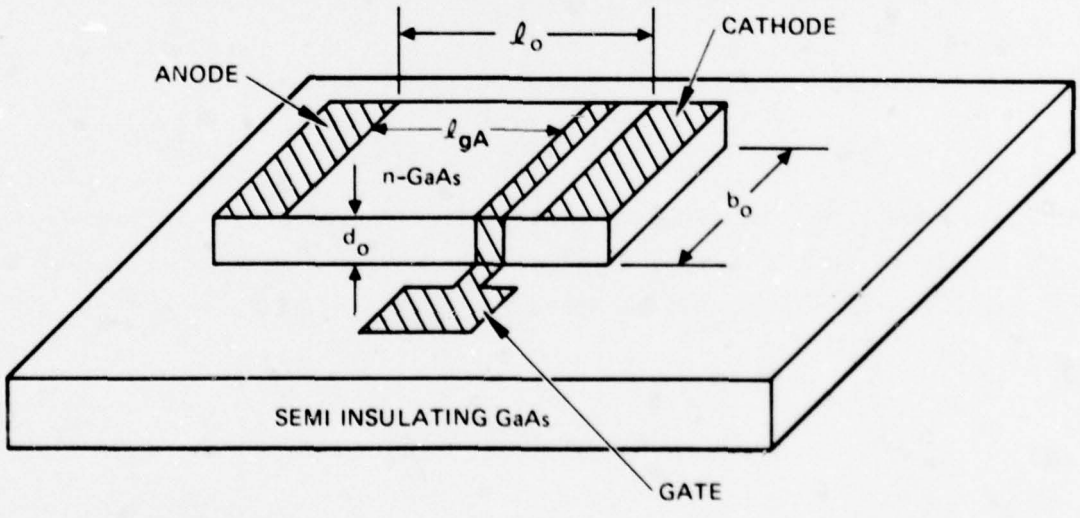

Figure 1. Planar structure of GaAs TELD.

A computer model has been developed that calculates the electrical characteristics of the TELD as a function of the device parameters and bias conditions. The calculation of the threshold condition follows the FET model by Pucel et al.[4] The TELD model shown in Figure 2 has been used to derive the threshold conditions under the gate of the TELD. A computer program that calculates the electric field under the gate and in the channel between the gate-cathode and gate-anode has been developed for designing the TELD. Once threshold conditions have been reached under the gate, the program calculates the steady-state conditions in the device assuming a mature domain has formed and is traversing the distance from the gate to the anode. The program calculates the electric field throughout the device, the current decrease caused by domain formation, and the voltage across both the device and a load resistor. The effects of doping density, channel depth, and load resistance can be investigated.

Following the derivation of Pucel et al.,[4] which makes use of Shockley's gradual channel approximation,[5] simple expressions can be derived for S, P, and I_{DS}[4,6] (Figure 3):

$$S = \sqrt{\frac{\phi - V_G}{W_o}} = l_c/d_o \qquad (3)$$

$$P = \sqrt{\frac{V_A + \phi - V_G}{W_o}} \qquad (4)$$

$$I_{AC} = \frac{G_o Z W_o}{L} \left[P^2 - S^2 - \frac{2}{3}(P^3 - S^3)\right], \qquad (5)$$

where

$$W_o = \frac{qN_D}{2\epsilon} d_o^2$$

ϕ = barrier height of the Schottky gate junction

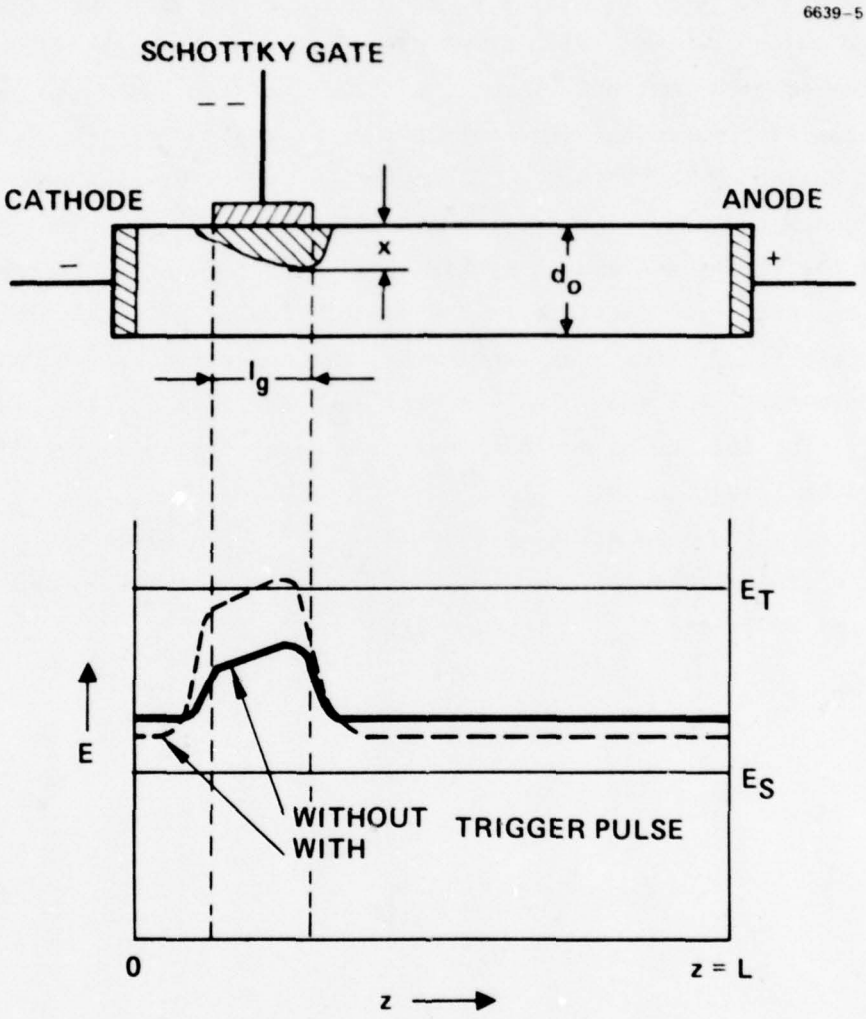

Figure 2. TELD electric field with and without trigger pulse for triggering domain.

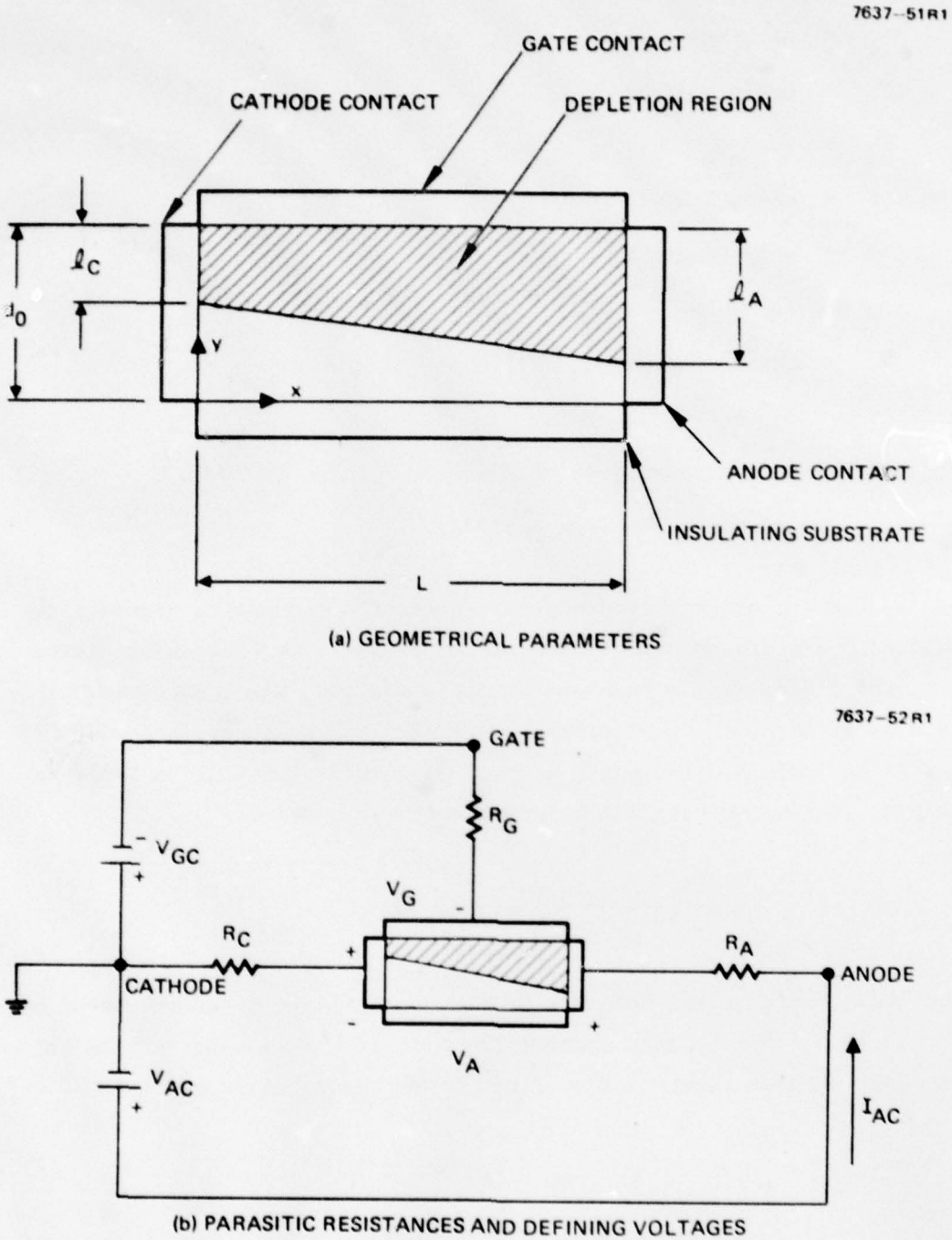

Figure 3. Cross-sectional diagram of TELD used in computer simulation: (a) geometrical parameters, (b) parasitic resistances and defining voltages.

V_g = gate voltage

V_D = drain voltage

$G_o \equiv q\mu_n N_D d_o$

Z = channel width

L = gate length

q = 1.6×10^{-19} C

N_D = doping density

ε = dielectric constant

d_o = active channel thickness

μ_n = low field electron mobility.

As the depletion region extends across the conducting channel, the longitudinal field in the channel will increase. In a normally biased TELD, the field will be greatest at the anode end, where the depletion width is greatest. Linear operation of the TELD will continue with increasing anode voltage until a critical velocity saturation field is reached. This condition is satisfied when

$$\frac{I_{AC}}{q\mu_n N_D Z d_o (1 - P)} = E_S \quad . \tag{6}$$

Once this condition has been reached, a domain forms under the anode edge of the gate. To take into account the parasitic resistance of the cathode and anode channel lengths, Eqs. 3 and 4 must be modified by

$$V_A = V_{AC} - I_{AC} (R_C + R_A) \tag{7}$$

$$V_G = V_{GC} - I_{AC} R_C \quad . \tag{8}$$

Making the appropriate substitutions into Eqs. 3 and 4 gives new expressions for S and P:

$$S = \sqrt{\frac{\phi - V_{GC} + I_{AC}R_C}{W_o}} \tag{9}$$

$$P = \sqrt{\frac{V_{AC} + \phi - V_{GC} - I_{AC}R_A}{W_o}} \tag{10}$$

All other relations remain unchanged.

These equations must be solved iteratively. For a given V_{AC} and V_{GC}, the corresponding I_{AC} is computed. This involves solving the transcendental equations, 5, 9, and 10, for linear operation. This task is easily accomplished by Newtonian interpolation. If the given relations can be rewritten in the form $f(I_{AC}) = 0$, a quadratically converging succession of approximations for I_{AC} is given by:

$$I_{AC_{K+1}} = I_{AC_K} - \frac{f(I_{AC_K})}{f'(I_{AC_K})} \quad , \tag{11}$$

where

$$f'(I_{AC_K}) = \left.\frac{df}{dI_{AC}}\right|_{I_{AC_K}} \quad .$$

Eq. 5 can be rearranged to give:

$$f(I_{AC}) = \frac{G_o Z W_o}{L}\left[P^2 - S^2 - \frac{2}{3}(P^3 - S^3)\right] - I_{AC} \quad , \tag{12}$$

with P given by Eq. 10 and S given by Eq. 9. Differentiating Eq. 12 yields

$$f'(I_{AC}) = \frac{-G_o Z}{L}\left[R_A + R_C - (PR_A + SR_C)\right] - 1 \quad . \tag{13}$$

These equations and an iterative procedure have been programmed on a microprocessor. For a given V_{gc}, the corresponding value of I_{AC} is calculated as a function of V_{AC}. The voltage V_{AC} is subdivided into equal steps from 0 to V_T, where V_T is the estimated threshold voltage. At $V_{AC} = 0$, the longitudinal field is zero and therefore $I_{AC} = 0$. Starting at this point, successive values of I_{AC} are computed using the interpolation formula given by Eq. 11.

The electric field in a TELD with a mature domain in transit can be derived if the velocity v versus electric field E characteristic is known. Following the derivation of Hartnagel,[7] in which a piecewise linear approximation for the v versus E curve is assumed as shown in Figure 4, one can show for $E_M < E_S$ that

$$(E_t - E_R)^2 \mu_o + (E_p - E_t)^2 \mu_n = (E_S - E_p)^2 \mu_n + 2(E_S - E_p)(E_M - E_S) \mu_n \tag{14}$$

and for $E_M > E_S$ that

$$(E_t - E_R)^2 \mu_o + (E_p - E_t)^2 \mu_n = (E_M - E_p)^2 \mu_n \quad . \tag{15}$$

These equations are based on the assumption that a mature domain has formed and, therefore, that the equal-areas rule applies. Eq. 14 has a factor of 2 which Hartnagel[7] does not show. From Figure 4, one can show the following relations:

$$(E_p - E_t) \mu_n = (E_t - E_R) \mu_o \tag{16}$$

$$E_S = E_t = v_t \frac{(1 - k)}{\mu_n} \tag{17}$$

$$v_t = \mu_o E_t \quad . \tag{18}$$

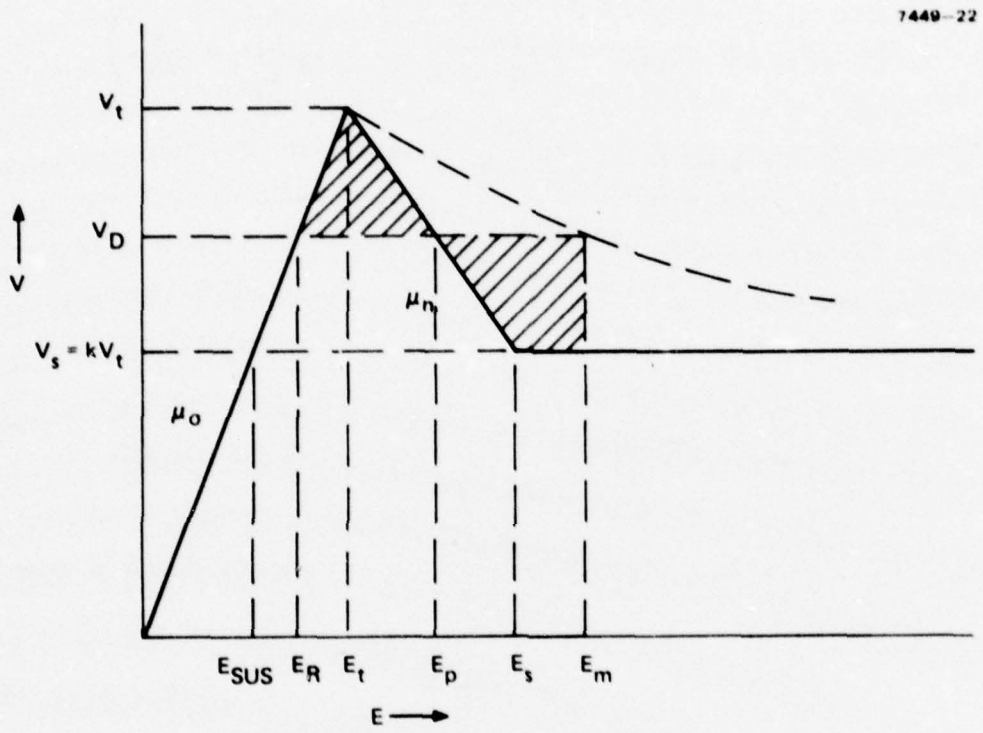

Figure 4. Piecewise linear approximation to the velocity versus electric field for GaAs.

After some manipulation, Eqs. 14 and 15 can be reduced to

$$(E_M - E_R) = \frac{(E_t - E_R)^2 \left(1 + \frac{\mu_o}{\mu_n}\right)}{2(E_R - kE_t)} - E_R\left(1 + \frac{\mu_o}{2\mu_n}\right) + E_t\left(1 + \frac{\mu_o}{\mu_n}\left(1 - \frac{k}{2}\right)\right) \qquad (19)$$

for $E_M > E_S$ and to

$$E_M - E_R = (E_t - E_R)\left[\left\{\frac{\mu_o}{\mu_n}\left(1 + \frac{\mu_o}{\mu_n}\right)\right\}^{1/2} + \left(1 + \frac{\mu_o}{\mu_n}\right)\right] \qquad (20)$$

for $E_M < E_S$. Using Eq. 19 or 20, the domain voltage is obtained from

$$V_D = \frac{(E_M - E_R)^2}{2qN_D} \quad . \qquad (21)$$

With the corrected version of the domain voltage, the steady-state conditions for a TELD with a domain in transit are calculated. Assuming a circuit similar to that shown in Figure 5, the current is related to the voltage by

$$V_{bias} = IR_L + V_{TELD} \quad , \qquad (22)$$

where

$$V_{TELD} = V_D + V_{gate} + E_R(\ell_{Ag} + \ell_{Cg}) \quad . \qquad (23)$$

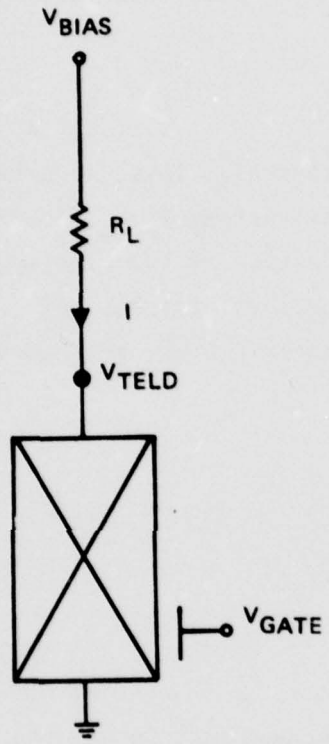

Figure 5.
Circuit for TELD and load resistor.

The distances from gate to anode and from gate to cathode are given by ℓ_{Ag} and ℓ_{Cg}, respectively. The voltage drop from the anode side to the cathode side of the gate is given by V_{gate} and is calculated by the Pucel[4] model. In addition, the current through the TELD must satisfy

$$I = q\mu_o N_D E_R b_o d_o \quad , \tag{24}$$

where $b_o d_o$ is the cross-sectional area of the channel. Thus, to determine the steady-state condition for a given bias voltage V_{bias}, load resistor R_L, and gate bias V_{gate} (which is a function of the bias applied to the gate), a self-consistent solution must be found for Eqs. 19 through 24. In comparison, before the domain is triggered, the conditions to be satisfied are

$$V_{bias} = I'R_L + V'_{TELD} \tag{25}$$

$$V'_{TELD} = V'_{gate} + E'_R(\ell_{Ag} + \ell_{Cg}) \tag{26}$$

$$I' = q\mu_o N_D E'_R b_o d_o \quad . \tag{27}$$

A computer program that runs on a microprocessor was written to solve these two sets of equations. The results of the program for the TELD and R_L as shown in Figure 6 are given in Table 1. The present form of the program calculates the conditions in the circuit before and after domain formation with a variable bias voltage that just satisfies the threshold condition for the given gate bias.

This model predicts a large current drop back since a mature domain is assumed to form immediately, resulting in a low value for the sustaining field in the drift region of the TELD. For the domain, which is nucleated under the gate, to transit from the gate to the anode, the field in this region must be large enough to sustain the domain. A first-order approximation to the sustaining field is that the current density in this region is greater than that obtained for the saturated drift velocity of the carriers. Referring to Figure 4, this implies that the field is greater than E_{sus} since

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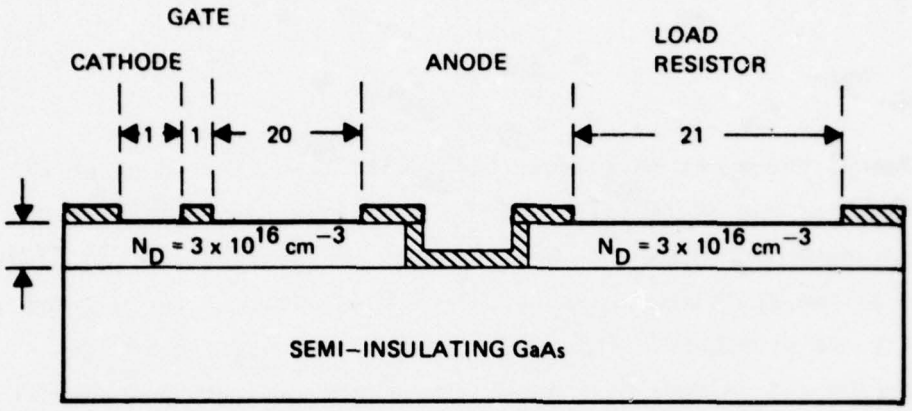

Figure 6. Schematic of TELD and load resistor (μ_n = 6000 cm^2/V_{sec}, E_T = 3.2 x 10^3 V/cm). Dimensions in micrometers.

Table 1. TELD Current and Voltage before and after Domain Formation

(R_L = 182 Ω, N_D = 3 x 10^{16} cm^{-3}, d_o = 2 μm, b_o = 20 μm)

V_{Bias}, V	V_{gC}, V	V_{TELD}, V		ΔV, V	I, mA		ΔI, mA
		Before	After		Before	After	
12.03	0	6.16	8.62	2.96	32.25	18.76	13.49
11.51	-1	5.90	8.09	2.19	30.82	18.78	12.04
11.12	-2	5.70	7.69	1.99	29.75	18.79	10.96
10.39	-4	5.34	6.96	1.62	27.72	18.83	8.89
9.81	-6	5.06	6.38	1.32	26.13	18.87	7.26

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$$J = qN_D E > qN_D v_{sat} \tag{28}$$

or

$$E > \frac{v_{sat}}{\mu_o} = E_{sus} \quad . \tag{29}$$

As the channel thickness decreases, the domain is nucleated under the gate for smaller and smaller V_{gs} and V_{AC} with lower and lower fields between the anode and the gate. For very thin channels (i.e., <0.5 μm), the field in the drift region is not above the sustaining value, and a domain will not propagate. This implies that, for a given Schottky-barrier height and channel doping density, there is a minimum channel thickness. If the depletion region X is normalized to the channel thickness d_o, then a maximum value for X/d_o is obtained as a function of doping density.

In addition to the requirements on the device geometry and material parameters determined by the model, the sensitivity of the field under the gate to the gate bias is also obtained. Trigger sensitivity is an important design and performance parameter in the operation of TELDs. Trigger sensitivity is defined as the minimum change of electric field required for domain formation due to a voltage applied to the gate. Sugeta et al.[8] defined the minimum field as that due to shot noise in the carrier density; however, as pointed out by Upadhyayula,[9] this definition does not lead to a useful device, since one would not want the TELD triggered by noise. Upadhyayula derived the trigger sensitivity including the load resistor in the anode circuit and showed that it is increased by $(1 + g_m R_L)$ due to the load resistor since it provides positive feedback. As the gate voltage is made more negative, the depletion region under the gate increases, which causes a smaller cross-sectional area for the current. This decreases the current, which in turn decreases the voltage drop across R_L. Since the bias is constant, device voltage increases, which increases the field under the gate. Thus, the feedback increases the field towards threshold. For the case with a cathode follower circuit, the feedback is negative.

The reverse bias on the gate, which determines the depletion width and therefore the current through the device, is the difference between the potential at the edge of the depletion region in the channel and the potential on the gate. Increasing the negative gate bias increases the reverse bias, which increases the depletion region. This in turn reduces the current and the voltage drop across the load resistor. As the voltage across R_L decreases, the cathode potential decreases. Thus, the potential of the depletion edge under the channel decreases, and the reverse bias between the channel and the gate decreases. Following the derivation of Upadhyayula, the current through the TELD is given by

$$I = (1 - X)\, \sigma E b_o d_o \quad , \tag{30}$$

where σ is conductivity.

The variation of field with gate voltage V_g is given by

$$\frac{dE}{dV_g} = \frac{E}{(1 - X)} \frac{dX}{dV_g} + \frac{g_m}{d_o b_o \sigma (1 - X)} \quad , \tag{31}$$

where

$$g_m = \frac{dI}{dV_g} \quad .$$

The depletion width for a given potential drop ϕ is

$$Xd_o = \sqrt{\frac{2\varepsilon\phi}{qN_d}} \quad . \tag{32}$$

The potential drop for the two cases (anode load resistor A and cathode follower CF) is

$$\phi_A = V_B - I(R_L + R_{ga}) - V_g + \phi_B \tag{33}$$

and

$$\phi_{CF} = \phi_B + I(R_L + R_{gs}) - V_g \quad , \tag{34}$$

where

V_B = bias voltage

R_{ga} = anode-to-gate channel resistance

R_{gc} = cathode-to-gate channel resistance

ϕ_B = built-in potential.

Evaluating dX/dV_g and substituting into Eq. 31 yields

$$\left.\frac{dE}{dV_g}\right|_A = \frac{-E(1 - g_m(R_L + R_{ga}))}{(1 - X)2X\phi_p} + \frac{g_m}{\sigma b_o d_o (1 - X)} \tag{35}$$

$$\left.\frac{dE}{dV_g}\right|_{CF} = \frac{-E(1 - g_m(R_L + R_{gc}))}{(1 - X)2X\phi_p} + \frac{g_m}{\sigma b_o d_o (1 - X)} \quad . \tag{36}$$

where ϕ_p is the pinch-off voltage.

Rearranging terms and using the relations $l_{ga}E = R_{ga}I - V_{ga}$ yields

$$\left.\frac{dE}{dV_g}\right|_A = -\frac{(1 + g_m R_L)E}{2X(1 - X)\phi_p} - \frac{g_m}{l_{ga}}\left[R_{ga}\left(\frac{V_{ga}}{2X(1 - X)\phi_p} - 1\right)\right] \tag{37}$$

$$\left.\frac{dE}{dV_g}\right|_{CF} = -\frac{(1 - g_m R_L)E}{2X(1 - X)\phi_p} + \frac{g_m}{l_{ga}}\left[\frac{R_{gc}V_{ga}}{2X(1 - X)\phi_p} + R_{ga}\right] \quad . \tag{38}$$

The last term in the parentheses in both equations is positive for most TELD designs, and, therefore, dE/dV_g is negative for the load resistor in the anode circuit but can be either negative or positive for the cathode follower case. Thus, the trigger sensitivity for the cathode follower case is decreased by $(1 - g_m R_L)$.

The computer model calculates the trigger sensitivity indirectly since the electric field under the gate at the anode edge is calculated as a function of gate bias for a given bias condition, doping density, device geometry, and load resistor. The electric field for the TELD described in Figure 6 with gate bias as a parameter is shown in Figure 7. Figure 8 plots the electric field under the gate at the anode edge as a function of the gate bias for this TELD and for a similar TELD with a doping density of 10^{16} cm^{-3}. The Nd_o and Nl_{gA} products for the two devices are given in Table 2 along with the trigger sensitivity and the corresponding gate trigger voltage to increase the field by 0.1 E_T. An optimum value[10] for V_g is between 0.5 and 1.5 V: if V_g is too small it will trigger spontaneously and if V_g is too large it will take too much logic swing and energy from the input to trigger the device.

Table 2. TELD Trigger Sensitivity

Doping Density, cm^{-3}	Nd_o, cm^{-2}	Nl_{gA}, cm^{-2}	$\Delta E/\Delta V_g$, cm^{-1}	ΔV_g, V
3×10^{16}	6×10^{12}	6×10^{13}	228	1.40
1×10^{16}	2×10^{12}	2×10^{13}	460	0.695

6325

The total current through the device consists of both the drift and displacement currents. As the electric field is raised to threshold from its bias value just below threshold, the conduction current increases. Once threshold is reached, a domain begins to form as the charge in the negative mobility region separates. As the charge redistributes itself, the field in the domain increases rapidly, resulting in an increase in displacement current that counteracts the decrease in conduction current due to the decrease in velocity. The net result is that the current remains relatively constant during the transition through the negative mobility region. The field outside the domain also remains nearly

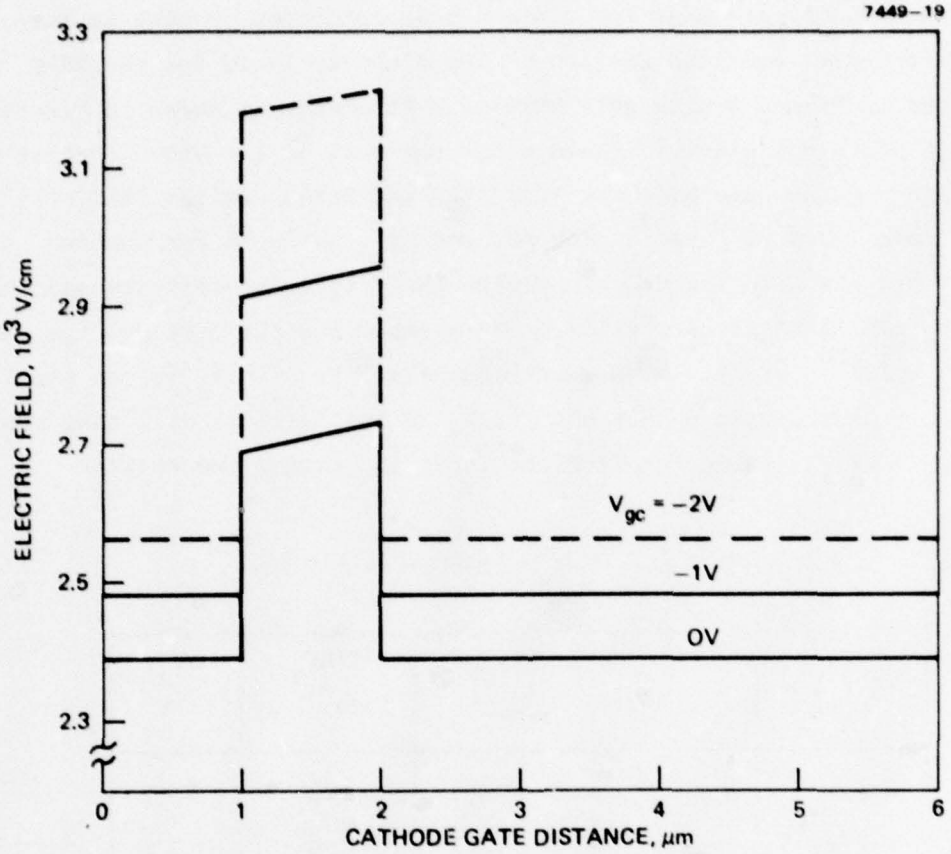

Figure 7. Electric field versus distance for TELD and load resistor in Figure 6 (V_{bias} = 11.1 V, I_{DS} = 29.75 mA).

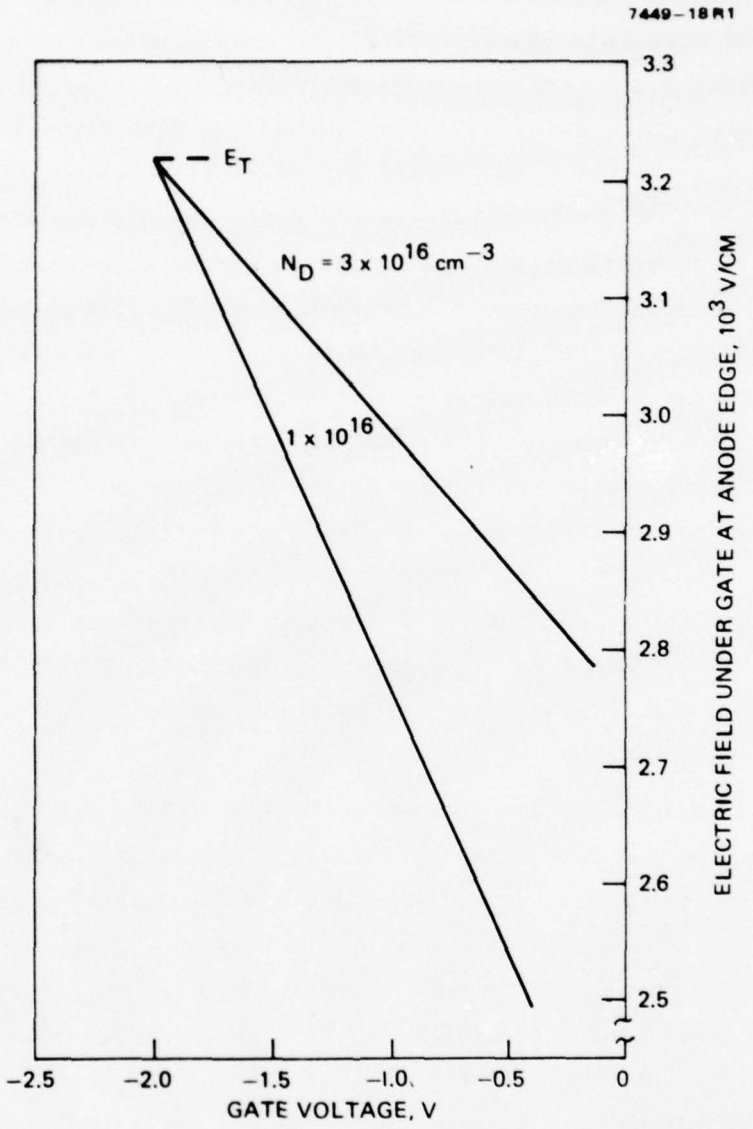

Figure 8. Electric field under the gate versus gate bias (R_L = 182 Ω, E_T = 3218 V/cm).

constant near threshold. Initially, the bias voltage that raises the field above threshold appears across the domain since the time constant associated with the negative dielectric relaxation time is less than 1 psec. Once the domain field has reached the positive mobility region, the field does not grow as rapidly and the total current, which corresponds to the conduction current in the domain, drops rapidly. The electric field drops outside the domain, causing a decrease in conduction current and a negative displacement current. The delay time is defined as the time required for the field to drop 50% of its total drop from the threshold value.

An approximate model, which can be used to investigate the effects of the circuit, characterizes the domain formation as the charging of the average domain capacitance through the low-field resistance and the load resistor.[7,11,12] This model includes the device and circuit parameters. The delay time for the domain formation is given by the RC time constant of the device and circuit, which corresponds to the time required for the field outside the domain to drop to one-half of its final low-field value.

The dynamic load line for the switching process described above is different from the load line for this simple model; however, the delay time for the two models is of the same form and differs by only a constant.[7] The advantage of the simple model is that circuit effects can be included, whereas, in the more exact model, circuit effects, especially parasitic capacitance, are difficult to take into account.

The response time of the TELD is a function of both the device and circuit parameters. To compare device and circuit parameters (e.g., doping density, device width, associated parasitics), a simple model is assumed for the device and circuit. As suggested by Hartnagel,[7] verified experimentally by Kuru et al.,[12] and investigated by Mause,[3] the domain formation time can be approximated by the time to charge the domain capacitance through the load resistor and low-field resistance. Including the effects of the parasitic capacitances, the equivalent circuit

for the device is as shown in Figure 9. The parastics are combined in C_T and the average domain capacitance is given by[7,13]

$$C_d = \left(\frac{3qN_D\varepsilon}{2E_{th}l_o}\right)^{1/2} b_o d_o \quad . \tag{39}$$

The response of the voltage across the device as its charges from threshold to a higher potential was calculated using the circuit analysis program SPICE. The results are shown in Figure 10 for a 10-μm-wide device with: $N_D = 1 \times 10^{16}$ cm^{-3}, parasitics corresponding to device-to-device spacings of 300 μm and 20 μm, and 2-μm-wide interconnecting lines. The effect of fan-out on device response can be seen from these results. As fan-out increases, interconnect capacitance increases along with additional gate capacitances of the next stage. Thus, C_T can be determined as a function of the fan-out. The effect of other loads can be taken into account in a similar fashion since the load resistance, as in the case of the interconnecting lines, is much smaller than R_L and can be neglected; only the increase in input capacitance needs to be considered. The effect of the load resistance on the response is also shown. In Figure 11, the response of a similar device with $N_D = 5 \times 10^{16}$ cm^{-3} and 300-μm and 20-μm spacings is plotted. A comparison between 10-μm- and 2-μm-wide devices is shown. If it is assumed that the switching time corresponds to the time necessary for the voltage to reach 90% of its final value, then

$$\tau_s \simeq 2.5\ R_L C_T \quad . \tag{40}$$

The load resistor is a function of low-field resistance and, therefore, of device geometry. Parasitic capacitance is a function of both device geometry and the spacing between devices. Switching time, as calculated by Eq. 40, is plotted for several different devices as a function of device spacing.

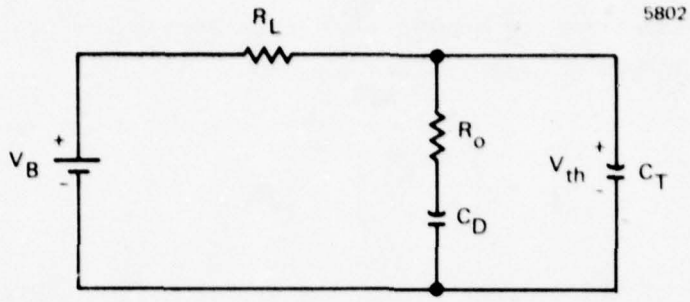

Figure 9. Equivalent circuit of TELD and circuit during domain formation.

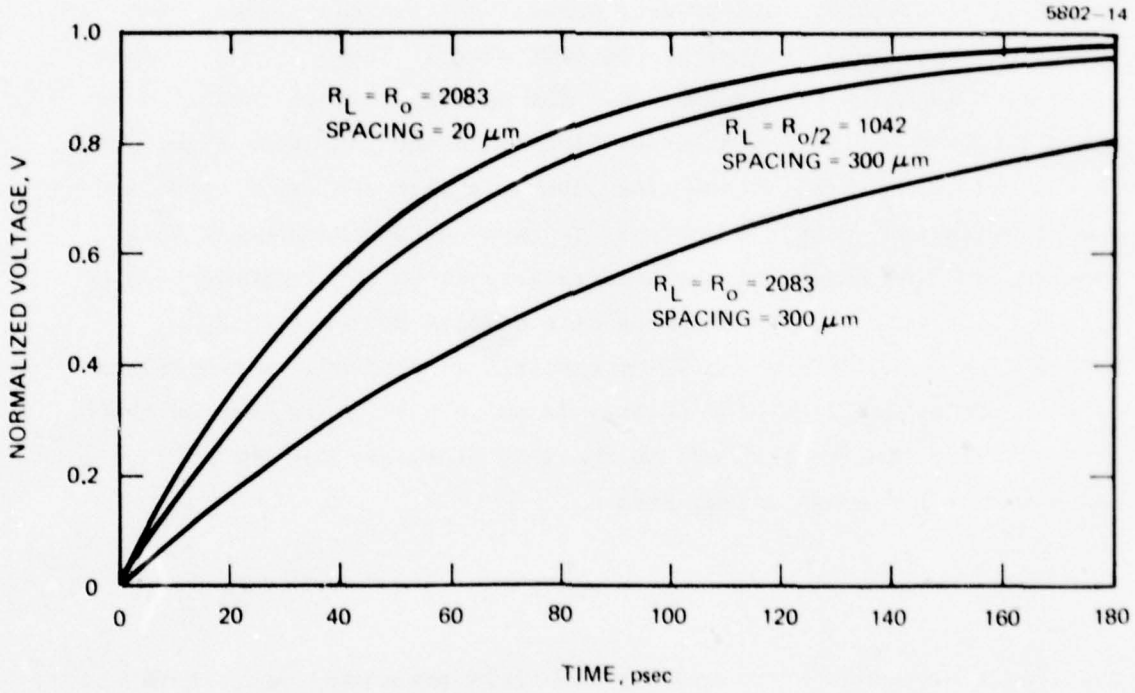

Figure 10. Response of device voltage versus time as a function of load resistance and device spacing (d_o = 10 μm, $N_D = 1 \times 10^{16}$ cm^{-3}).

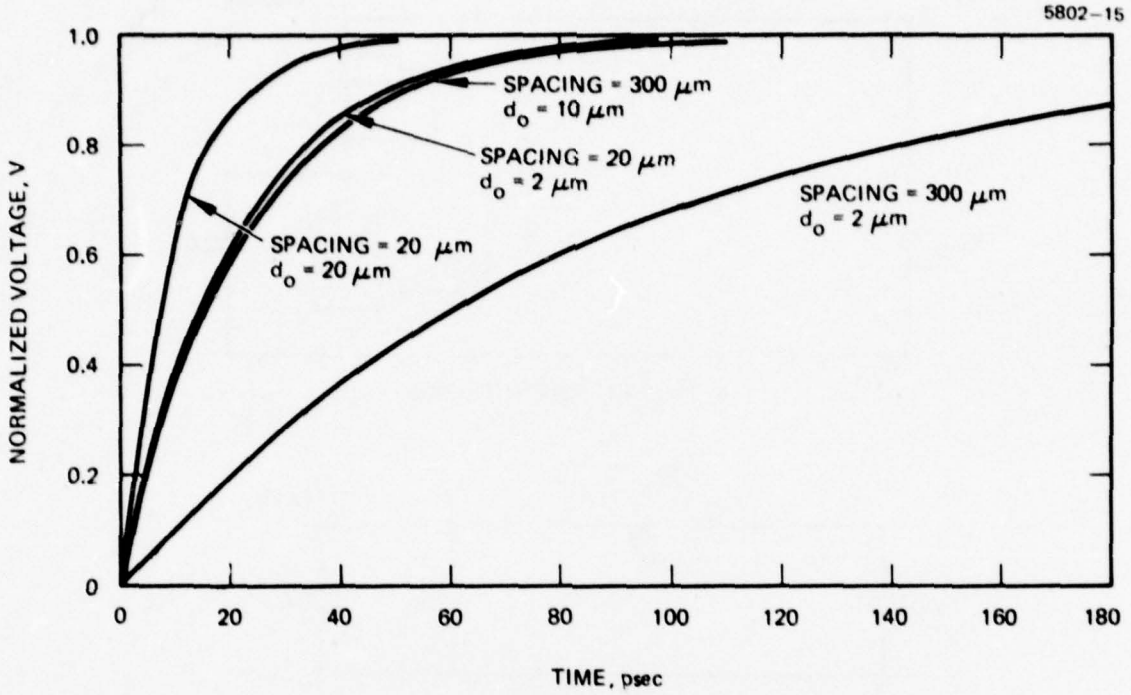

Figure 11. Response of device voltage versus time as a function of device width and spacing ($R_L = R_o = 416\ \Omega$, $N_D = 5 \times 10^{16}\ cm^{-3}$).

By incorporating an active load (such as an FET) instead of a load resistor, the power consumption can be reduced. The circuit is shown in Figure 12 along with the equivalent circuit for the TELD below threshold. In the equivalent circuit, the fringing capacitance of the FET has been neglected, and the FET is assumed to be a constant current source. The load line for this circuit is shown in Figure 13 with the two states of the TELD depicted. Point A represents the I and V across the TELD below threshold; point B represents the I and V with a domain in the transient. The change in voltage Δ at the anode of the TELD corresponds to the logic swing or pulse output of the circuit. The time constant or switching time is given by

$$\tau_d \equiv R_o C_T \quad . \tag{41}$$

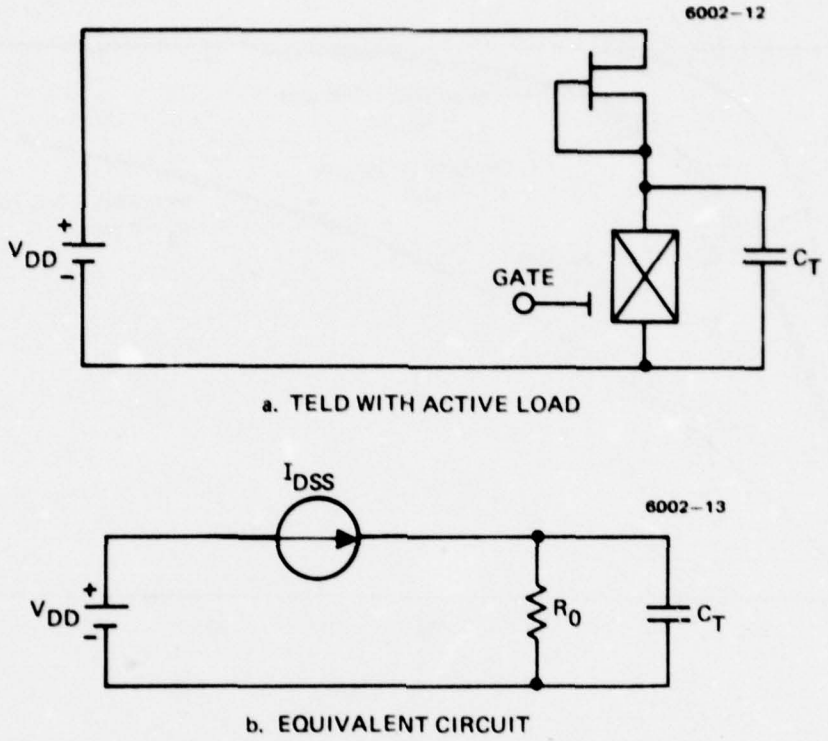

Figure 12. TELD with active load bias just below threshold.

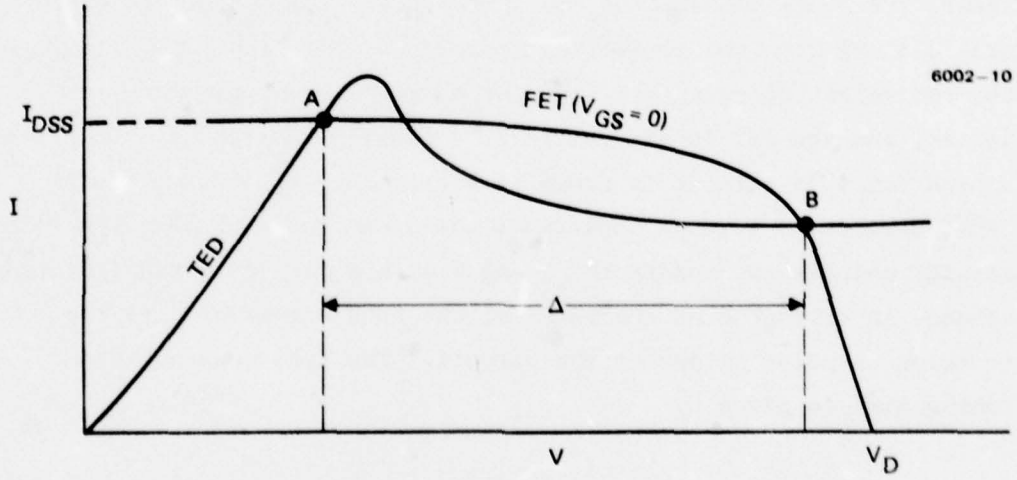

Figure 13. Load line for active load.

To compare this with the case of resistive loading, consider Figure 14. For the switching time and power dissipation to compare with case 1, the active load case R_L must be equal to R_o (case 2) but the logic swing Δ must be much smaller. For much larger R_L (case 3), the logic swing corresponds to the active load; however, the switching time and power dissipation are much larger. For R_L smaller than R_o, the device is faster and the circuit dissipates less power; however, the logic swing goes to zero.

When the domain reaches the anode and is collected, the voltage across the TELD decreases as the voltage drop across R_L increases. With no domain in the TELD, the equivalent circuit shown in Figure 9 reduces to the circuit in Figure 15. The time for the voltage across R_o to decay back to just below threshold is given by

$$\tau \simeq 2.5\ (R_L/R_o)C_T \quad . \tag{42}$$

Thus, the decay time is normally one-half (i.e., $R_L = R_o$) or less of the domain charging time. In an actual device (as explained above), the domain nucleates much faster at first than this simple model predicts; thus, it is possible that a new domain will be initiated since the anode voltage remains too large, causing the field in the device to be above threshold.

A means of avoiding this self-triggering is to couple the output of the TELD via a MOS capacitor pick-off probe mounted on the TELD, as shown in Figure 16. The insulated gate responds to both the formation and extinction of the domain and the domain passage under the gate. This structure has been used for function generators because the output of the gate is a function of the gate geometry.[14,15]

The device structure shown in Figure 17 consists of a uniform TELD with a thin dielectric layer and a nonuniformly shaped metal electrode on it. Assuming that the electric field in the dielectric is perpendicular to the sandwich and that the displacement current is much smaller than the TELD current, the potential distribution in the TELD

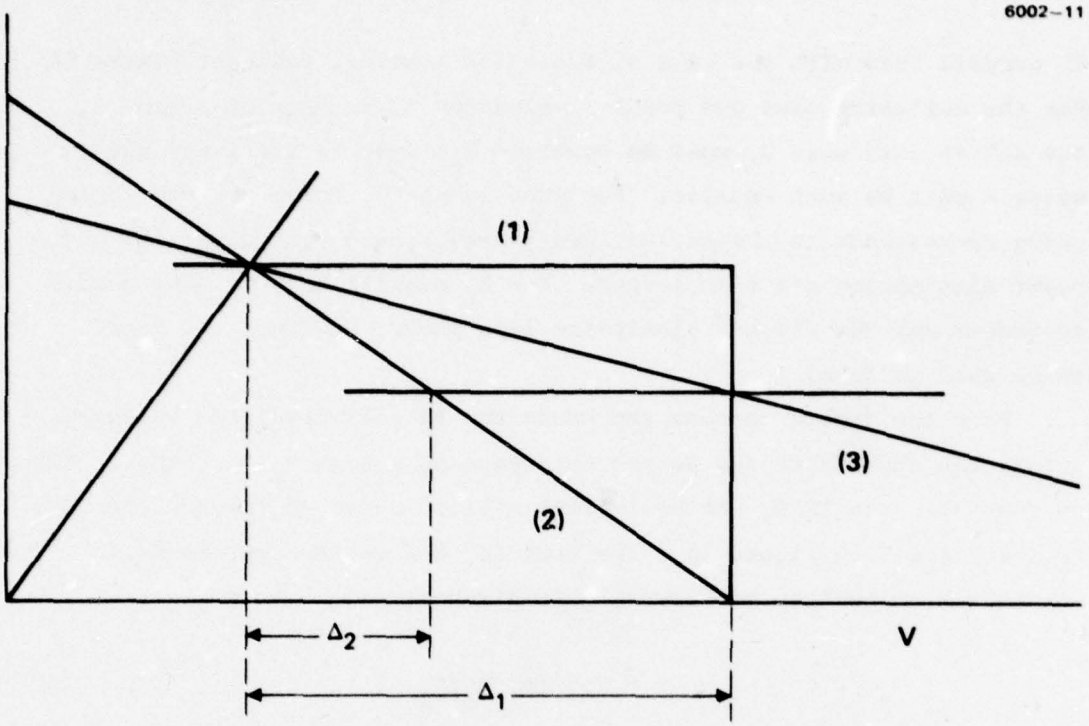

Figure 14. Comparison of load lines for FET load and different load resistors.

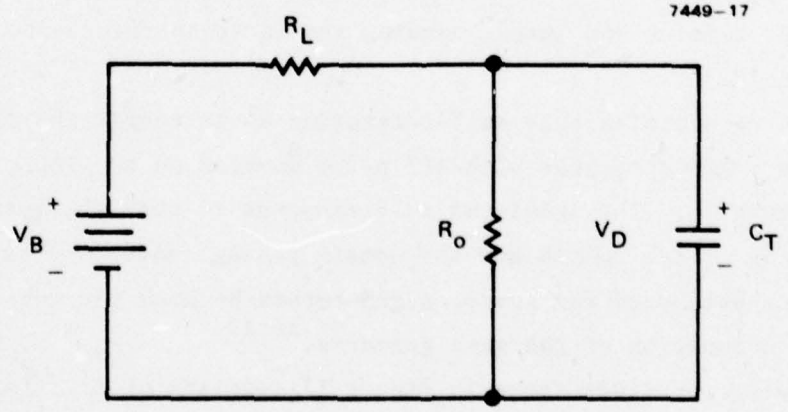

Figure 15.
Equivalent circuit of TELD and circuit after domain collection. (V_D = voltage across TELD with domain in transient).

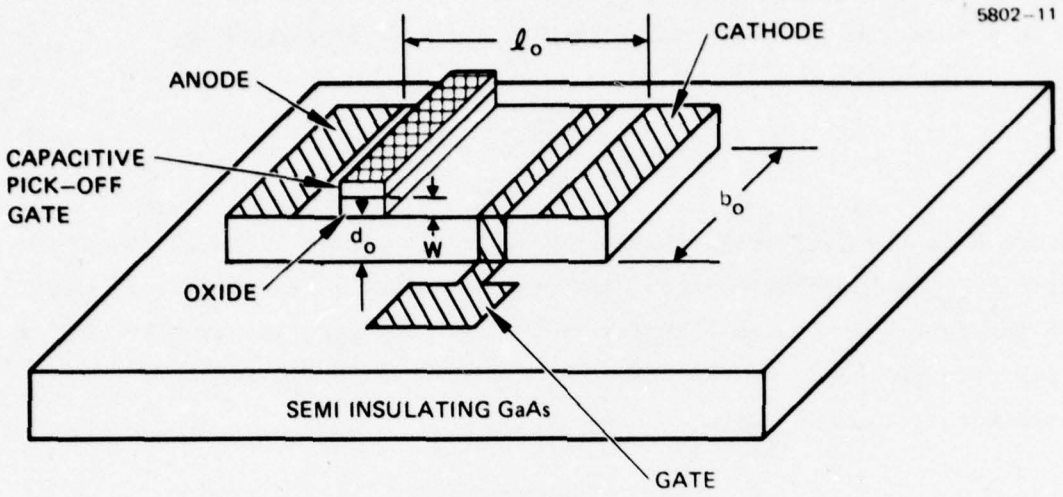

Figure 16. Planar structure of GaAs TELD with capacitively coupled pick-off gate.

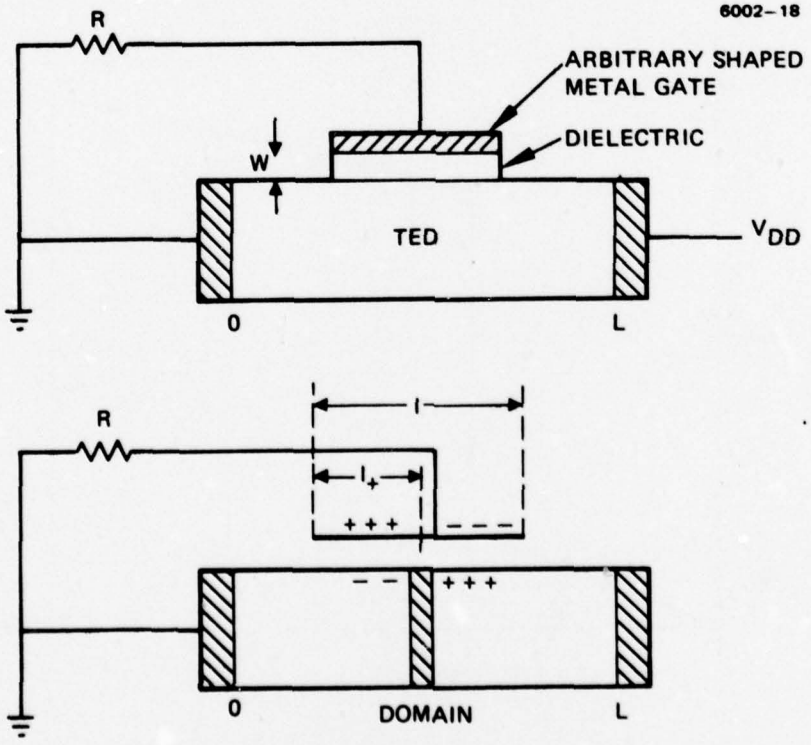

Figure 17. TELD with arbitrarily shaped insulated gate.

will be as shown in Figure 18. As the domain moves under the gate from x to x + dx, the induced charge on the plate is increased by

$$\Delta Q_m = \frac{\varepsilon V_{ex}}{W} f(x)dx \quad , \tag{43}$$

where W is the dielectric thickness, ε is the permittivity of the dielectric, V_{ex} is the domain excess voltage, and f(x) is the arbitrary width of the gate. Since the charging current of the gate is given by the time rate of change of the charge and since the domain velocity v_D is constant, it follows that

$$I = \frac{\varepsilon V_{ex}}{W} f(v_D t)v_D \quad . \tag{44}$$

Thus, the current of the insulated gate while the domain is passing under it is given by a constant multiplied by the arbitrary gate width.

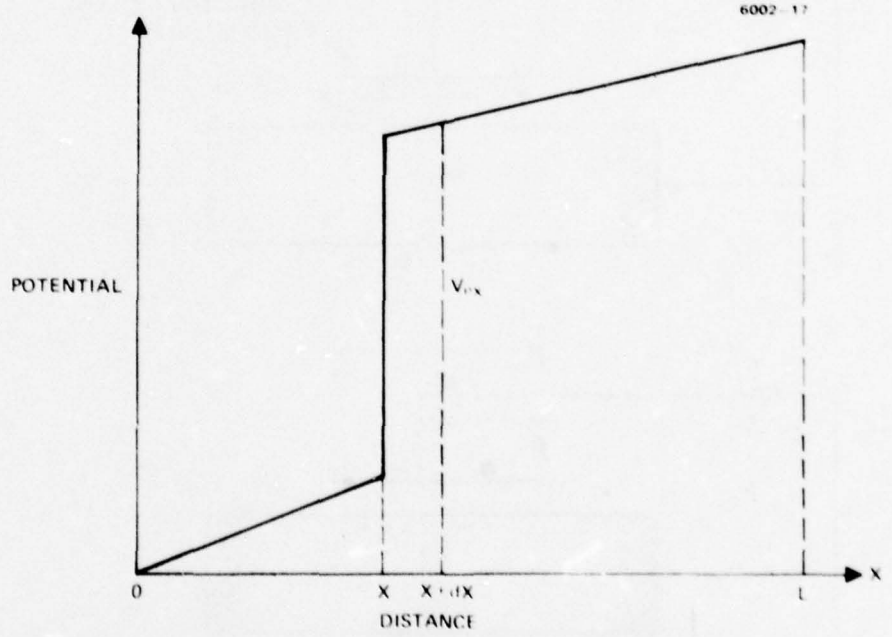

Figure 18. Potential distribution versus device length.

In addition to the induced current during domain transit, the gate has large capacitive transients when the domain is formed at the cathode or at another gate and collected at the anode. The rise time of these spikes is the same as the rise time or domain formation time discussed previously. The magnitude of the pulse is a function of the capacitance of the insulated gate.

The current output of the gate pickup can be used to trigger other TELDs. The current pulse collected during the passage of the domain under the gate is delayed in time from the input by the transit time of the domain to the gate, whereas the current pulse generated by the domain formation is delayed only by the domain formation time. However, if a domain is in transit, then the TELD is inhibited and no new domain may be initiated and, therefore, the output must wait until the domain is collected before responding.

Two factors must be considered in the design of the coupling circuit between the MOS pick-off gate and the input to a TELD or an FET. First, the pulse amplitude and the charging time of the input of the next device must be such that the succeeding device will respond. For the case with a rectangular pick-off gate, the current is given by

$$I = \frac{\varepsilon V_{ex} l_{pg} v_{sat}}{W} \quad , \tag{45}$$

where l_{pg} is the length of the pick-off gate, and the domain velocity has been approximated by the saturated velocity. The equivlanet circuit for the TELD and succeeding stages is shown in Figure 19. The pick-off gate has been assumed to be close to the anode so that the device resistance between the gate and the anode has been neglected. The capacitance of the succeeding gate is represented by C_g, and a bias resistor is provided for discharging this capacitor. For the next stage to be triggered, the voltage V_i must reach 1 V as quickly as possible. The RC time constant of this charging circuit is given by

$$\tau = R_B C_g \quad . \tag{46}$$

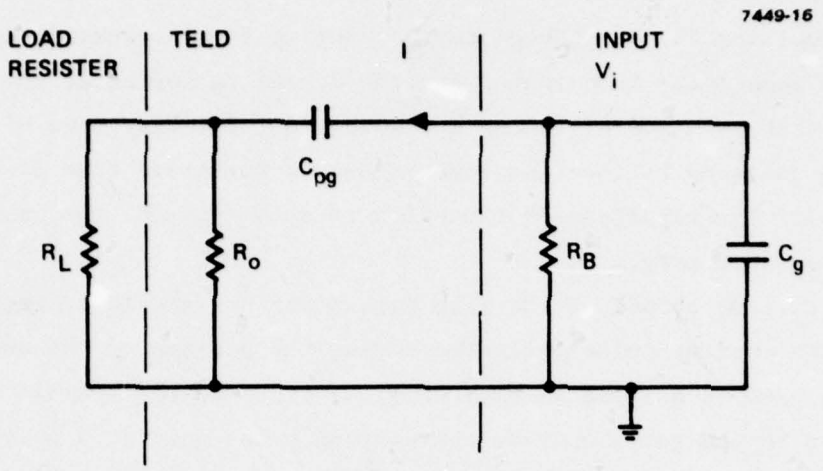

Figure 19. Equivalent circuit of MOS pick-off gate and input to next stage.

For V_i to reach 1 V,

$$1 = IR_B \tag{47}$$

so that

$$\tau = \frac{C_g}{I}$$

$$\cong b_o l_g \sqrt{\frac{N_D}{10^{17}}}\ 10^{-7}\ \frac{W}{V_{ex} b_o v_{sat}} \quad . \tag{48}$$

For a doping density of 2×10^{16} cm^{-3}, $l_g = l_{pg} = 1$ μm, an oxide thickness of 500 Å, and a device width of 20 μm, the discharge time constant is

$$\tau = 6.3\ \text{psec}/V_{ex} \quad , \tag{49}$$

To ensure that the input gate discharges before the domain is collected, the discharge time constant is given approximately by

$$\tau \cong R_B(C_g + C_{pg}) \quad , \tag{50}$$

which, for the above case, yields

$$\tau \approx \frac{W}{\varepsilon V_{ex} b_o v_{sat}} \left[b_o l_g \sqrt{\frac{N_D}{10^{17}}}\ 10^{-7} + \frac{\varepsilon b_o l_g}{W} \right]$$

$$\approx 16.3\ \text{psec}/V_{ex} \quad . \tag{51}$$

Thus, for normal excess domain voltages near 1 V, both the charging time and the discharging time are appropriate. The value for the bias resistor is given by

$$R_B = 706/V_{ex} \quad , \tag{52}$$

which is a reasonable value. With the capacitively coupled pick-off gate, the capacitance loading the anode consists only of the device itself and not the interconnect lines and fan out. Therefore, the time constant for the anode voltage to decay to a value below threshold after the domain has been collected is greatly reduced and self-triggering can be eliminated.

Another advantage of the capacitively coupled pick-off gate is that it is ac coupled to the next stage and therefore does not require level shifting between stages. This reduces power consumption and circuit complexity.

As discussed above, the speed of the TELD is limited by the parasitic capacitance of the device and circuit. The RC time constant of the associated circuitry can cause additional domains to be nucleated, and the TELD will remain in a memorized state.[10] To optimize the design of the device parasitics and the circuit layout, an accurate calculation of the parasitic capacitance between the different contacts and the capacitance to ground of each has to be performed.

The parasitic capacitance is analyzed by first obtaining a Green's function appropriate for the conductor configuration. The charge distribution on the conductors and the total charge are obtained by incorporating the Green's function with a numerical approach (e.g., method

of moments). Finally, from the total charge on each conductor, the self-capacitance (capacitance to ground) and the mutual capacitance (capacitance between conductors) is calculated.

SECTION 3

PROCESSING TECHNOLOGY

Planar TELDs have been fabricated in ion-implanted, LPE and VPE GaAs wafers. Devices such as those shown in Figure 20 have been made by photolithography with 1-μm-long Schottky-barrier gates. In addition, GaAs anodic oxide has been grown on test samples.

Several experiments have been performed to establish an implantation process suitable for TELD fabrication. Nominal goals for this work were to establish an implant process with Nd products greater than 2×10^{12} cm^2. The implant depth is limited by the maximum accelerating voltage, which, for our implant apparatus, is 275 kV. To avoid impact ionization on the one hand and large variations in activation due to compensation on the other, we chose 5×10^{16} cm^{-3} as a reasonable carrier concentration.

Three series of experiments were carried out to investigate the influence of ion source, ion dose, and anneal temperature on the resulting implant. In all cases, silicon ions were used to avoid subsequent diffusion during anneal. In the initial experiment, doubly ionized implants were performed at 550 keV energy. Based on the experimental range-energy curve of Figure 21, the expected depth of these implants is approximately 5000 Å. All implants were capped with CVD SiO_2 and annealed in flowing hydrogen. The results of these implants were evaluated using a universal material evaluation mask. Patterns on this mask were used for standard C-V profiling as well as for contact-resistance and Hall-mobility measurements. Rough estimates of the activation percentage and mobility were obtained from the contact resistance data by comparing the low field resistance of a contact resistance pattern (after subtracting the contact resistance component) to the saturated current obtained from the same pattern. The result of these experiments are summarized in Table 3. The results of these experiments were comparable except that the profiles were significantly

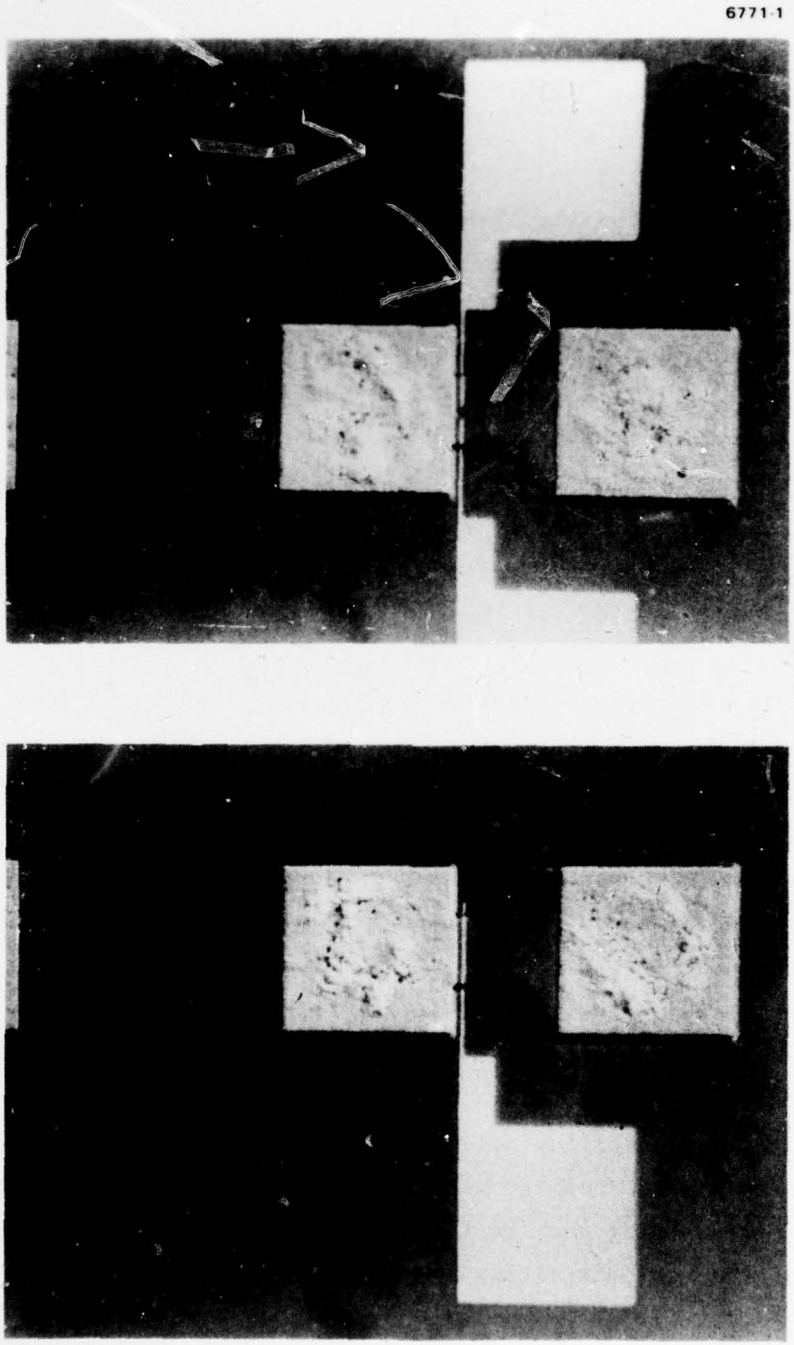

Figure 20. Single- and dual-gate TELDs.

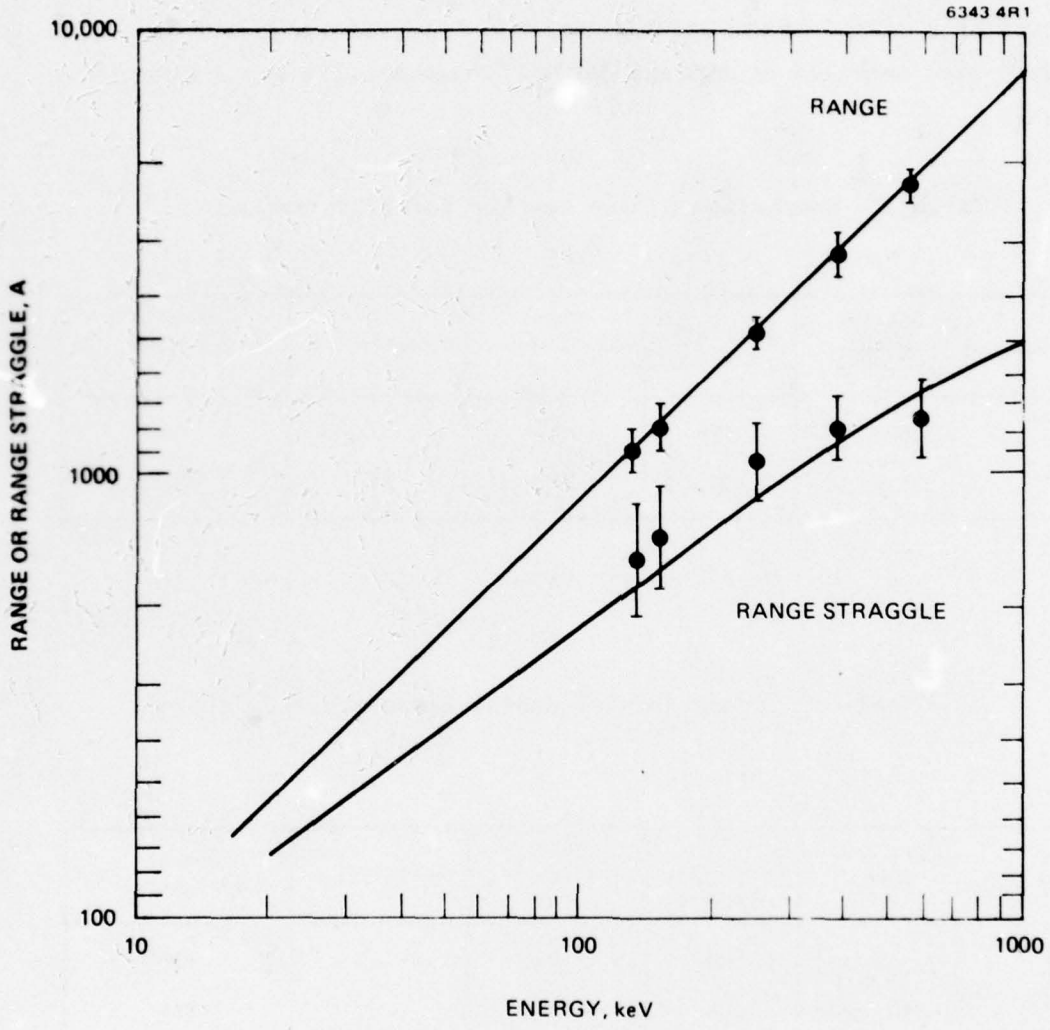

Figure 21. Range and range straggle for Si → GaAs.

different. Specifically, the SiH_4 implant indicated some possibility of surface conversion. To check for the possibility of nitrogen contamination in the doubly ionized beam (Si^{++} has the same e/m ratio as N_2^+), a series of singly ionized 275 keV implants was performed, and the implants were annealed at 800 and 860°C. These results are summarized in Table 4.

Table 3. Comparison of Ion Species for TELD Implants

Ion Source	550 keV Dose, cm^{-2}	Mobility, $cm^2/Vsec$	Sheet Resistance, Ω/sq	Activity, %	Anneal Temperature, °C
SiF_4^{28}	3.5×10^{12}	4528	760	53	860
SiH_4^{28}	3.5×10^{12}	4901	580	74	860

6325

Table 4. Comparison of Anneal Temperatures

Ion Source	275 keV Dose, cm^{-2}	Mobility, $cm^2/Vsec$	Sheet Resistance, Ω/sq	Activity, %	Anneal Temperature, °C
SiH_4^{29}	3.5×10^{12}	3600	940	48	800
SiH_4^{29}	3.5×10^{12}	5300	1100	—	860
SiH_4^{28}	3.5×10^{12}	3225	880	60	800
SiH_4^{28}	3.5×10^{12}	3765	660	71.4	860
SiF_4^{28}	3.5×10^{12}	3500	920	51.4	800
SiF_4^{28}	3.5×10^{12}	3805	560	80	860

6325

The available beam current at SiH_4^{29} was very low and thus confusing results were expected from those implants. The remaining four implants behaved as expected. No apparent differences between the different ion sources were observed. The mobility and activation of the higher temperature anneals are higher, as expected. The most noticeable difference was with implant profiles, as shown in Figure 22. These results show a higher than expected surface doping level after the 860°C anneal.

Though the I-V characteristics exhibited a threshold voltage and a current drop back when dc tested in wafer form, as shown in Figure 23, the devices would not oscillate when mounted in an rf test circuit. Two possible reasons for this problem might be that (1) the activation of the implanted dose is poor for low doses, resulting in a lower than anticipated doping density with many deep traps, and (2) the depletion region under the Schottky-barrier gate when normalized to the depth of the implant (~0.3 to 0.4 μm) is large. The first reason would result in a low value for the Nd product, less than 10^{12} cm^{-2}. The second reason would mean that the field outside the gate region is too small to sustain the domain once it has formed under the gate.

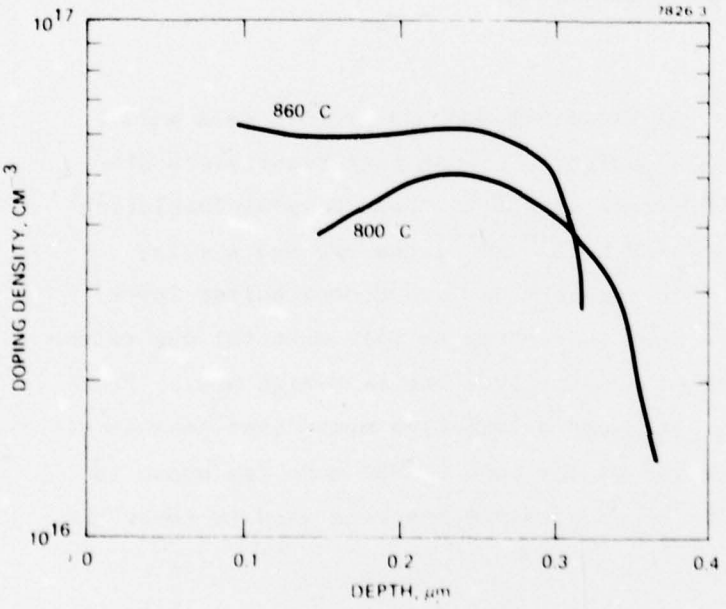

Figure 22.
Doping density versus depth for two different annealing temperatures.

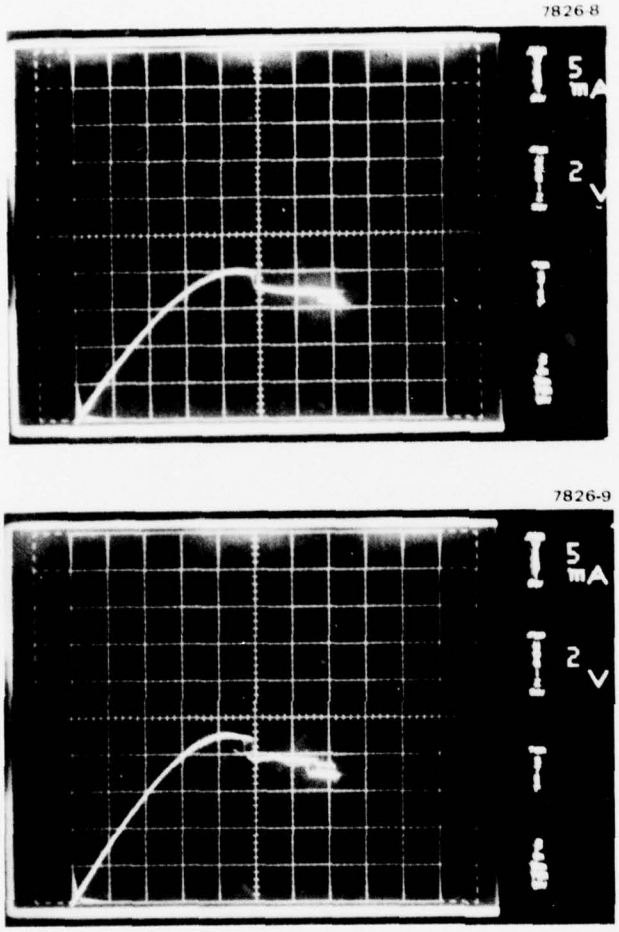

Figure 23.
Typical I-V characteristics for ion-implanted TELDs.

Devices fabricated on HRL-grown LPE GaAs and on VPE GaAs with buffer layers have operated as designed. These test results are discussed in Section 4. The LPE was 2 μm thick, grown on semi-insulating GaAs with a doping density of 2.9×10^{16} cm^{-3}; the VPE had similar doping density and channel thickness but was grown on a buffer layer. Only two terminal TELDs have been fabricated on this material due to the difficulty in defining a 1-μm-long gate over the 2-μm-high mesa. Problems with depositing a 1-μm gate over a 2-μm-high mesa exist because of the thinning of the photo-resist at the edge of the mesa (as shown in Figure 24). Even though 1 μm of photoresist has been used to cover the

wafer, the photo-resist at the edge of the mesa has thinned down to less than 0.5 μm. When a 1-μm-long, 0.5-μm-high gate is deposited, the gate metal will not be well defined over the mesa edge and will often break when the photoresist is removed. In addition, it is difficult, due to interference effects, to define a 1-μm gate with contact photolithography both on top of the mesa and on the substrate.

Wafers have been processed with 2-μm-high mesas and gates defined by E-beam lithography. In Figure 25, the metal gate, which is 7500 Å long and 4000 Å thick, is shown to have excellent continuity over the 2-μm-high mesa. The TELD mask set has been modified to deposit bench marks on the wafer so that alignment of the E beam can be made and 1-μm gates can be deposited.

Gallium arsenide anodic oxide has been grown at HRL with both aqueous and nonaqueous liquid electrolytes. Oxide grown with solutions of inorganic salts in organic solvents has been found superior to oxide grown with aqueous solutions. In particular, nonaqueous electrolytes appear generally to yield oxide/GaAs interface properties that are less sensitive to atmospheric humidity. Consequently, subject to compatibility with other process requirements, nonaqueous electrolytes will be used for oxide growth.

Incorporating anodic oxide MIS structures as GaAs IC elements presents some unique fabrication problems. Oxide must be grown on device mesas that are electrically isolated on high-resistivity substrates. Substrate resistance essentially prevents oxide growth unless, as a minimum requirement, the wafer is illuminated to excite photoconductivity. Growth is still extremely nonuniform if only edge contact is made to the wafer. Growth of a uniform oxide requires a large-area contact to the back of the wafer. The voltage drop through the substrate is then sufficiently low to ensure a uniform oxide. A proprietary, nondestructive technique for supplying the necessary back contact has been developed at HRL. In combination with illumination, this technique has been demonstrated to permit rapid growth of anodic oxide on high-resistivity material and a very uniform oxide over a region that conforms to the area of the back contact.

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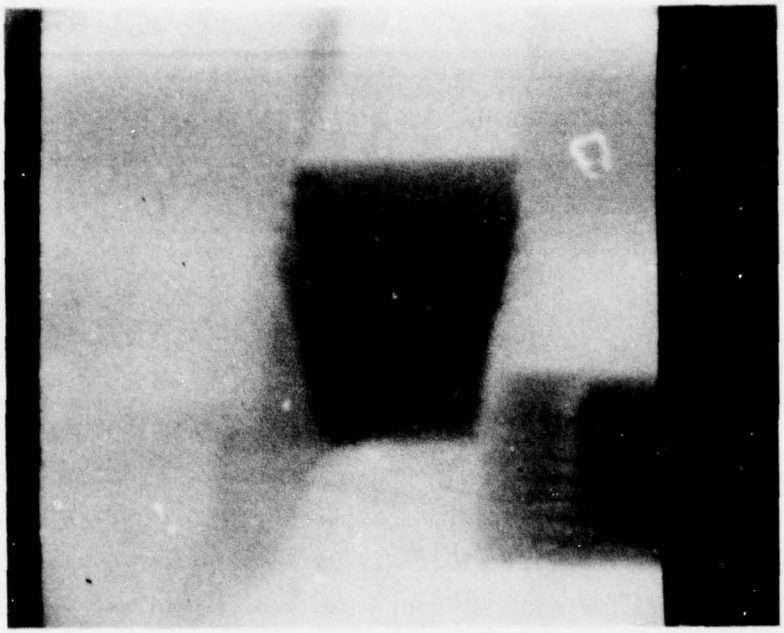

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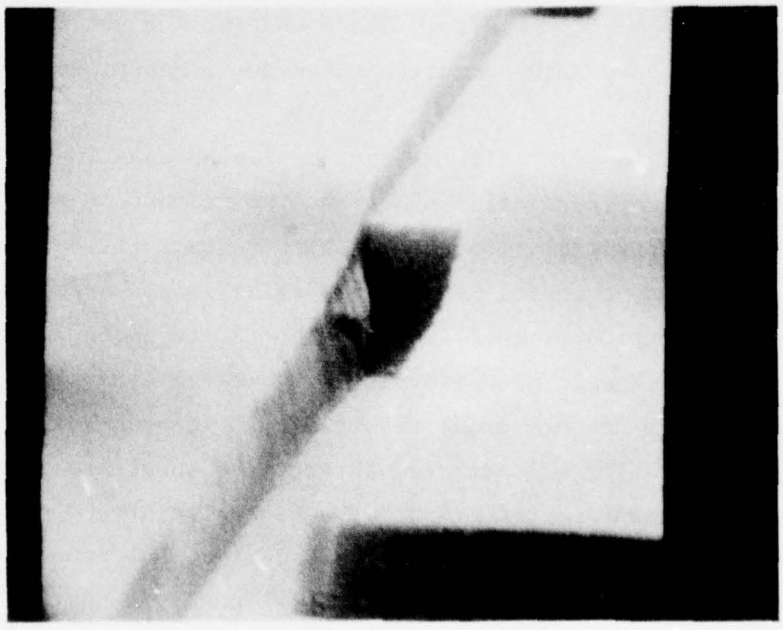

Figure 24. SEM photographs showing gate pattern on 2-μm-high mesa with 1 μm of photoresist.

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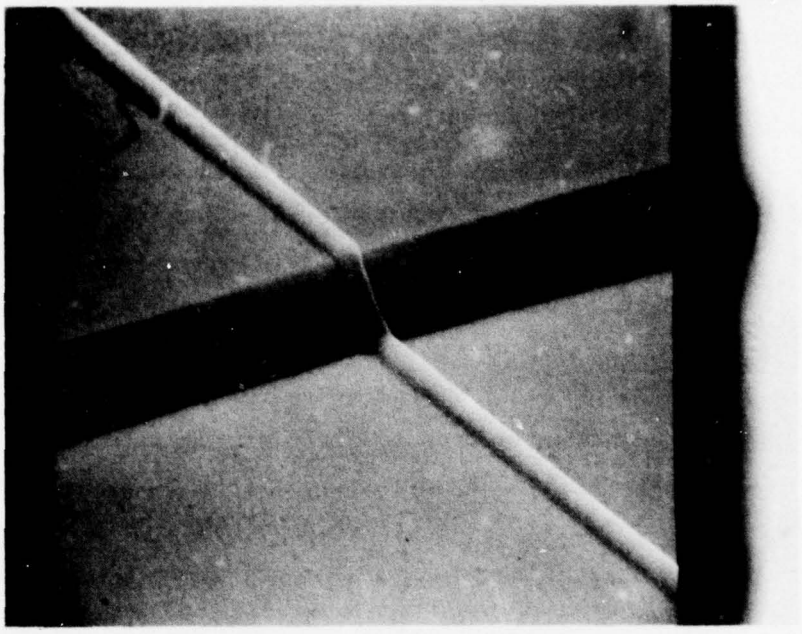

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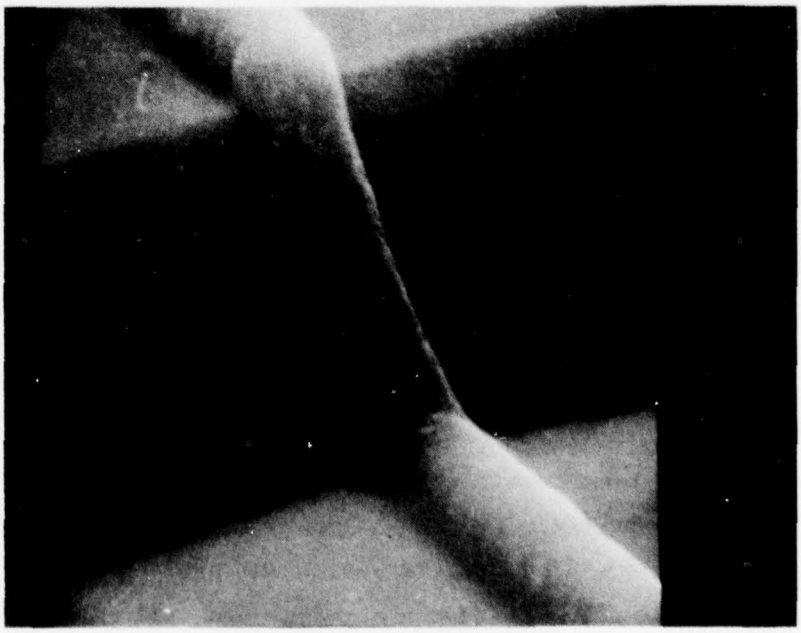

Figure 25. SEM photographs of 2-μm-high mesa with 7500-Å-long by 4000-Å-high gate deposited by E-beam lithography.

The intrinsic chemical vulnerability and thermal instability of the oxide place constraints on device design and fabrication. Anodic oxide is readily soluble in even moderately strong acids and bases. In particular, the oxide rapidly dissolves in the alkaline developer for conventional positive photoresist. As a result, the oxide is damaged by the photolithographic processing necessary to pattern the overlaying metalization. Patterning the oxide by etching is also difficult since (1) resist development and oxide etching occur with the same chemical treatment, and (2) the oxide etch rate is so high that undercutting is difficult to control.

An alternative fabrication technique that appears quite feasible is to use a single photoresist step to both control selective oxide growth and pattern the overlaying metal by lift-off. We have observed that oxide growth can be readily restricted to openings in a coating of positive photoresist. The extent of lateral growth depends on the post-development bake treatment of the resist and anodic growth parameters. Lateral growth can be limited to less than 1 μm for an oxide thickness of 0.1 μm. Following oxide growth, the desired metal layer is deposited and patterned by dissolving the photoresist with organic solvents. The solvents used do not attach the anodic oxide. Clearly, this technique requires a device design in which both the oxide and the overlaying metal have the same pattern. Direct contact of the metal to the GaAs is prevented by the lateral growth of the oxide. We expect that a nonanodizing metal lying on the high-resistivity substrate can also be exposed during anodization without significantly affecting oxide growth on the mesas.

The completed anodic oxide MIS structure remains vulnerable to chemical attack and thermal degradation, and the fabrication process must be designed to accommodate this vulnerability. If further chemical processing is essential, the MIS elements are best encapsulated with a deposited, impervious dielectric. Subsequent processing temperatures are limited to about 350°C by the onset of anodic oxide decomposition, which results in the loss of As and the crystallization of the remaining Ga_2O_3. Interface properties degrade with the onset of crystallization.

A test pattern for our anodic oxide (800 Å thick) is shown in Figure 26. The scale represents 1.48 μm/div.

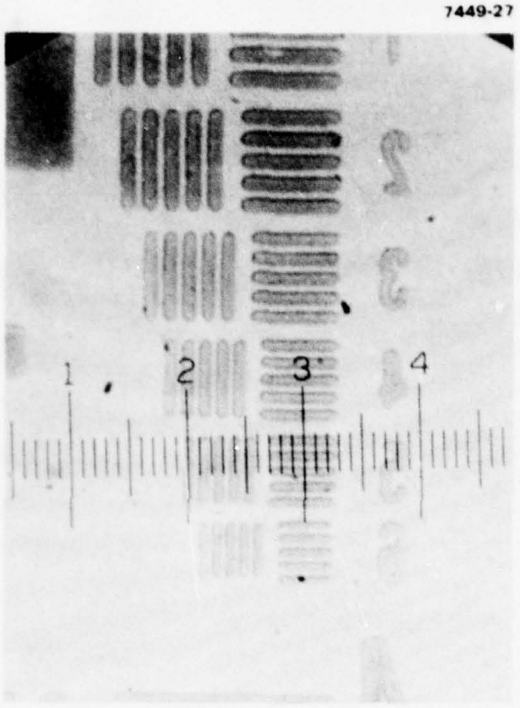

Figure 26. Test pattern for anodic oxide on GaAs.

SECTION 4

DEVICE EVALUATION

The I-V characteristics of the gateless LPE TELD (shown in Figure 27) exhibit 24% current drop back. Similar results were obtained for the VPE TELDs. These devices were mounted in the coplanar waveguide circuit shown in Figure 28 and tested in the test setup shown in Figure 29. Initially the devices were biased above threshold to determine their transit time frequency, which, for the VPE and LPE devices, was between 2.75 and 3.0 GHz. A spectrum is shown in Figure 30 for the LPE TELD. The characteristics of the oscillator for a VPE TELD are shown in Figure 31. This corresponds to a mobility of ≈5500 cm^2/V-sec or a domain velocity of ≈8.8 x 10^6 cm/sec.

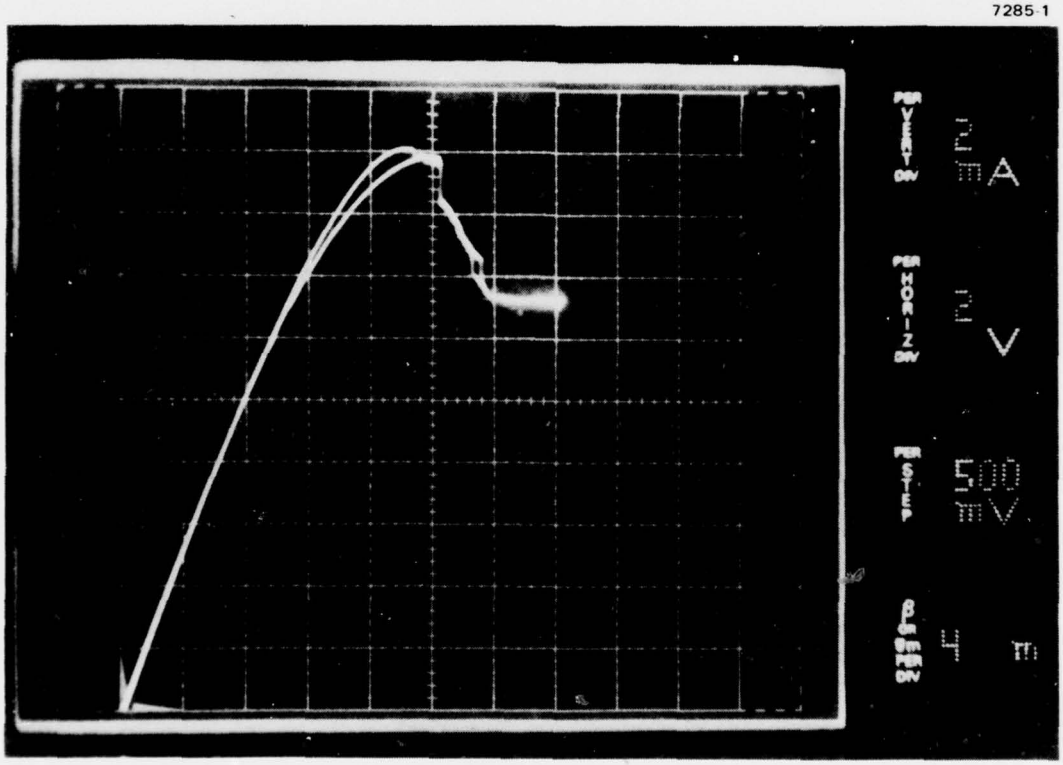

Figure 27. I-V characteristics of gateless TELD made with HRL-grown LPE GaAs.

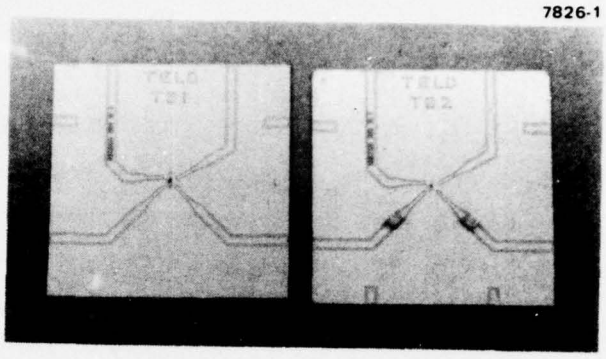

Figure 28. TELD test boards.

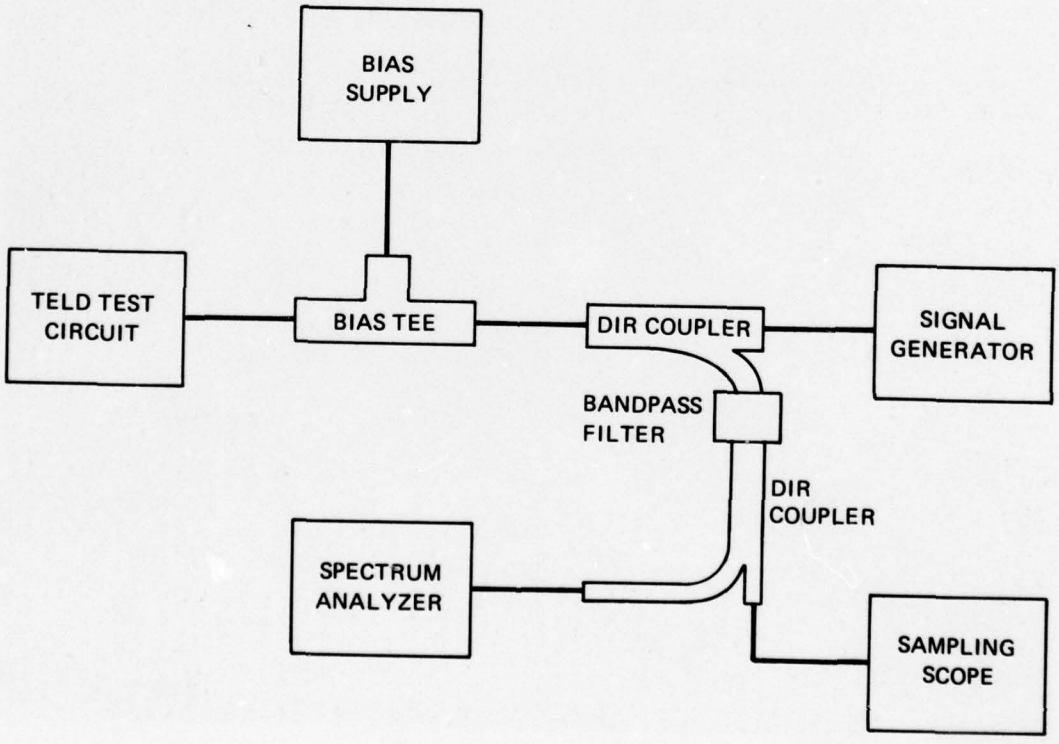

Figure 29. RF test setup for TELDs.

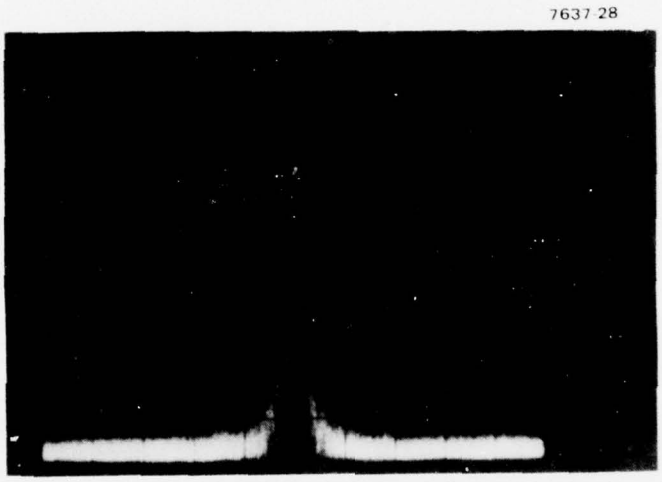

Figure 30.
Spectrum of TELD transit time frequency (f_o = 2.94 GHz, vertical = 10 dB/div, horizontal = 1 MHz/div, V_{bias} = 11.1 V, I_D = 14.4 mA).

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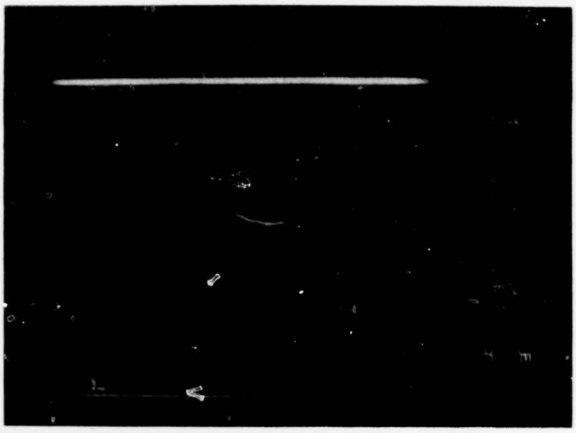
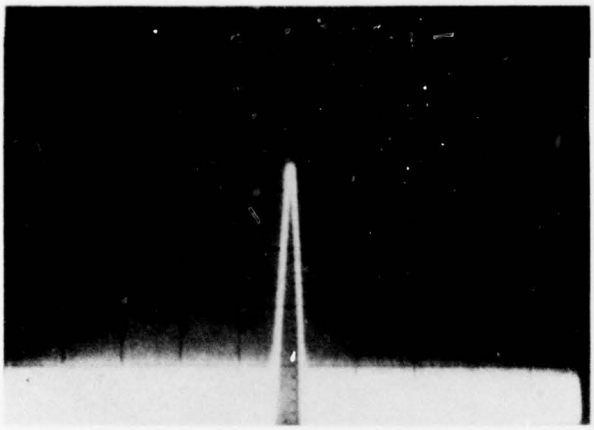
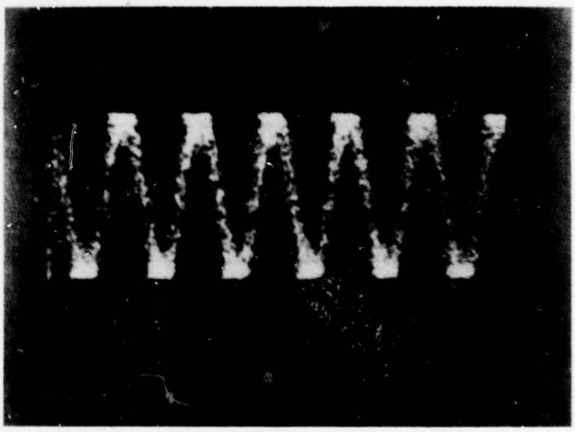
PHOTOMICROGRAPH OF TWO TERMINAL TED
WITH RESISTOR LOAD (210 x)



DC I–V CHARACTERISTICS OF TED



SPECTRUM OF SELF-OSCILLATION MODE
V_T = 8.87 V I_T = 11.9 mA f_o = 3.01 GHz
(H – 1 MHz/DIV V – 10 dB/DIV)



TED WAVEFORM – SELF-OSCILLATION MODE
(H – 200 PS/DIV V – 50 MV/DIV)

Figure 31. Two-terminal TELD characteristics.

In addition to the transit time frequency, the TELD could also be tuned to oscillate at a much lower frequency — approximately one-third the transit time frequency. The spectrum is shown in Figure 32. Both the LPE and VPE TELDs with buffer layers exhibited this low-frequency oscillation; however, it was much easier to obtain in the LPE than in the VPE TELDs. A possible explanation for this low-frequency oscillation is that it is the result of dielectric loading on the domain by the substrate.[10] An explanation for the low-frequency oscillation is not readily available. The effect of the interface states between the active region and the bulk GaAs must, due to the difference between nonbuffered LPE TELDs and the buffered VPE TELDs, have some effect.

The TELDs have also been tested as frequency dividers by injecting a signal at two and three times the transit time frequency. With the devices biased slightly below threshold, we were able to trigger the device and obtain output at one-half (in the first case) or one-third (in the second case) the input signal. For the divide-by-two circuit, an instantaneous bandwidth at the input frequency of 80 MHz was obtained, and the TELD could be tuned to divide by two from 5.2 GHz to 5.6 GHz. The output spectrum for the divide-by-two case is shown in Figure 33. Trigger sensitivity measurements were not made. The threshold voltage was 10.4 V at just over 17 mA, and, with an input signal amplitude of just under 1 V, the device was triggered and divided the input signal by two. For the divide-by-three circuit, the input frequency was 8.25 GHz, and the instantaneous bandwidth at the input frequency was 30 MHz. For this setup, the circuit also divided by nine, resulting in an output frequency of 0.917 GHz (transit time frequency = 2.75 GHz). For this case, all the harmonics were present and 20 dB down from the input signal except for the transit time frequency, which was only 2 dB down in amplitude. For a similar device with a transit time frequency of 2.365 GHz, the input and output waveforms for the divide-by-three case are shown in Figure 34.

By retuning the circuit, the TELD divided by 2, 3, or 5 down to the low-frequency oscillation of 1.077 GHz. The input and output waveforms for the three cases are shown in Figure 35.

7826-2

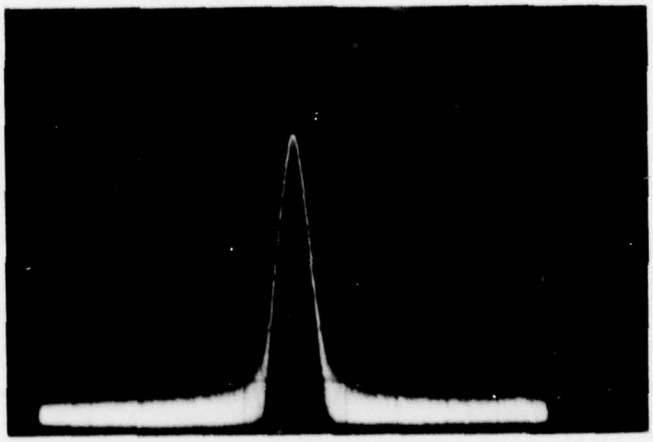


Figure 32.
Spectrum of TELD low-frequency oscillation (f_o = 1.001 GHz, vertical = 10 dB/div, horizontal = 500 kHz/div, V_{bias} = 11.1 V, I_D = 14.5 mA).

7637-3

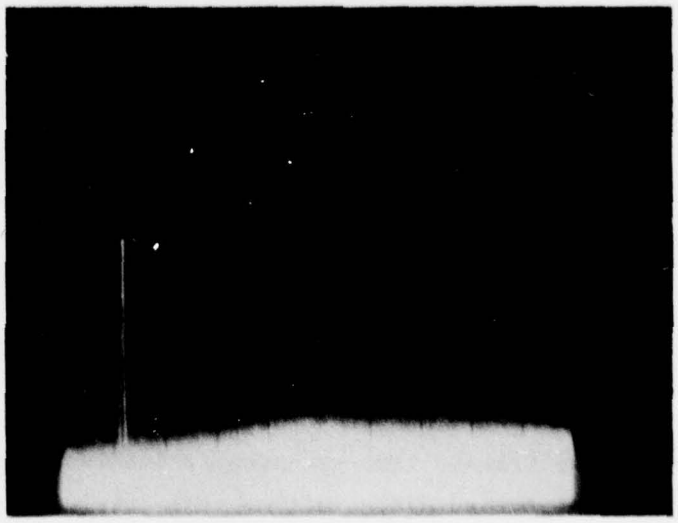


Figure 33.
Output spectrum for divide-by-two TELD (2.720 $\leq f_o \leq$ 2.769 GHz, V_{bias} = 10.13 V, I_D = 17 mA).

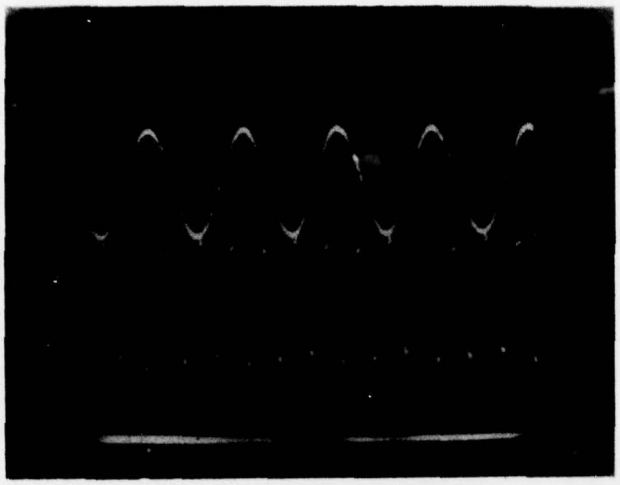


Figure 34.
Output waveform of divide-by-three TELD (f_{in} = 7.095 GHz, f_o = 2.365 GHz).

Using the modified mask set, which incorporates bench marks for the E-beam machine, gates were deposited over the mesas by E-beam lithography. Scanning electron microscope pictures of a single-gate, a dual-gate, an input-output gate TELD, and a five-stage delay circuit are shown in Figure 36. The gate length is 0.5 μm. Since the height is 0.5 μm, the mesa as shown is approximately 3 μm high. The I-V characteristics for two adjacent devices, one without and one with a gate, are shown in Figure 37. The threshold current and voltage for the gateless device is 20 mA at 9.4 V. The corresponding threshold conditions for the gated device are 18.4 mA at 8.4 V. Figure 37 also shows the effect of a negative bias on the gate. The corresponding threshold conditions are listed in Table 5. The I-V characteristics for the dual-gate TELD are shown in Figure 38. In Figure 38(a), 0 V is applied to gate 2 while gate 1 is stepped from 0 to -8 V. In Figure 38(b), gate 2 has -4 V on it and gate 1 is stepped from 0 to -8 V. It would be possible to obtain a set of bias voltages on the anode and gates 1 and 2 such that the TELD would operate as either an OR gate or as any AND gate.

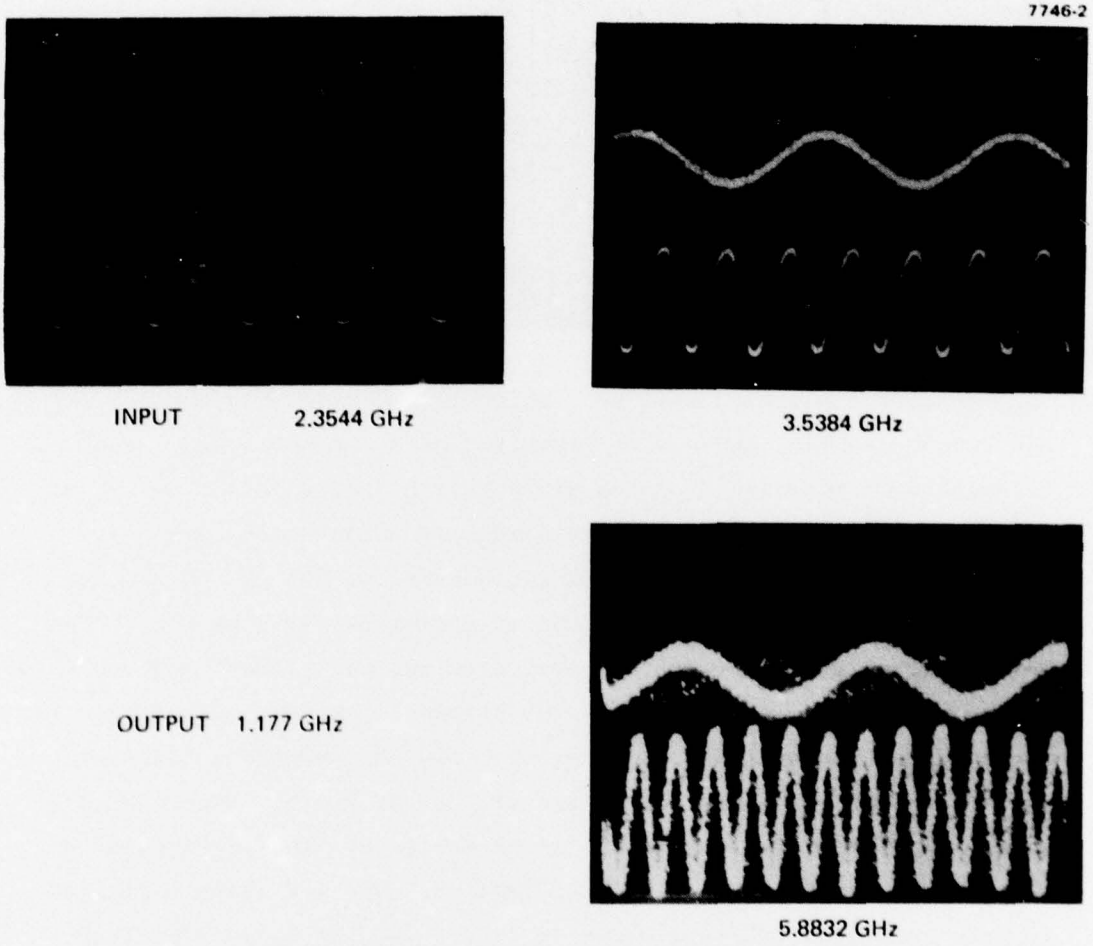
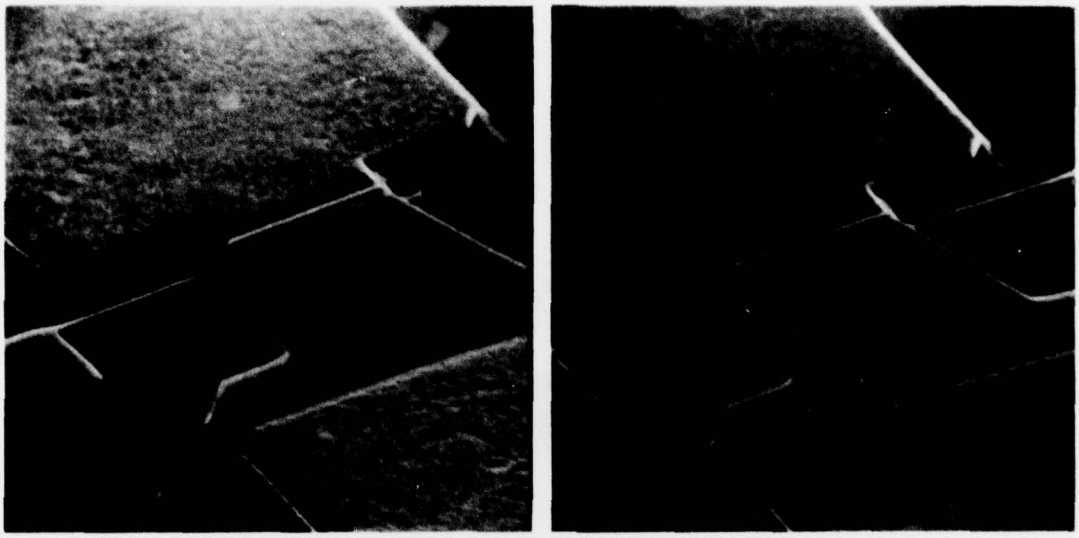
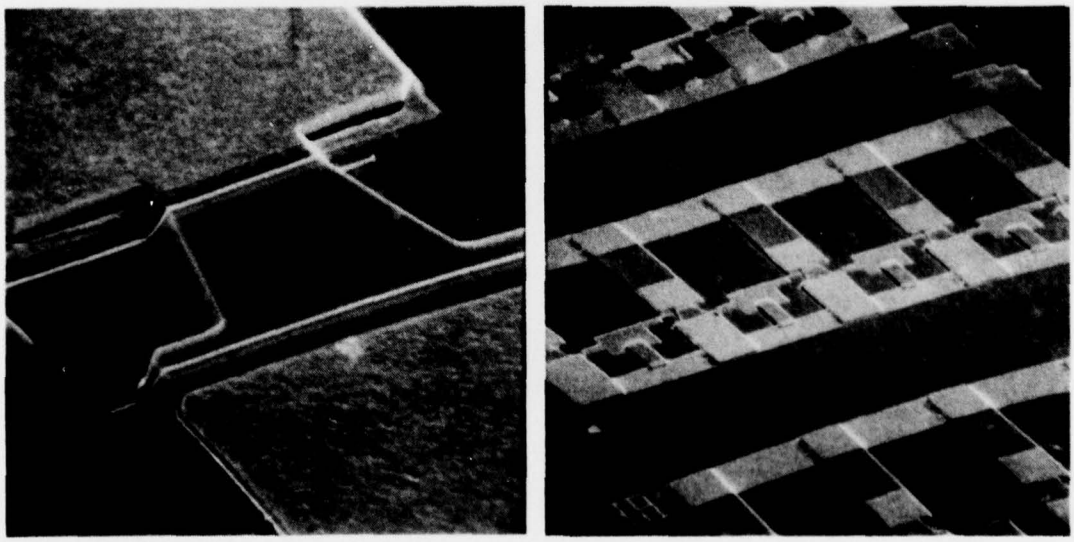


Figure 35. TELD frequency division.



(a) SINGLE GATE

(b) DUAL GATE

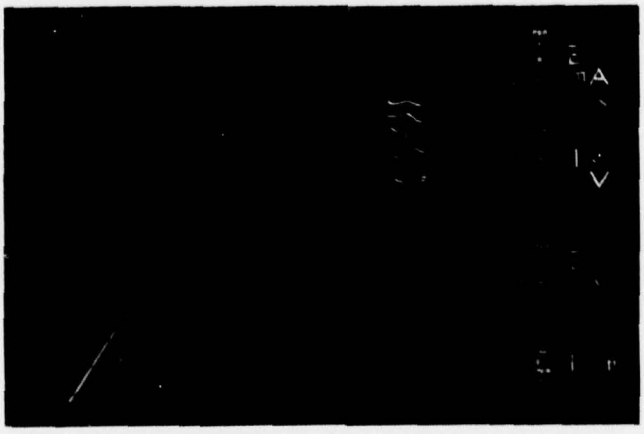


(c) INPUT-OUTPUT GATE

(d) 5-STAGE DELAY CIRCUIT

Figure 36. SEM photographs of TELDs with gates defined by E-beam lithography.

(a) TWO TERMINAL



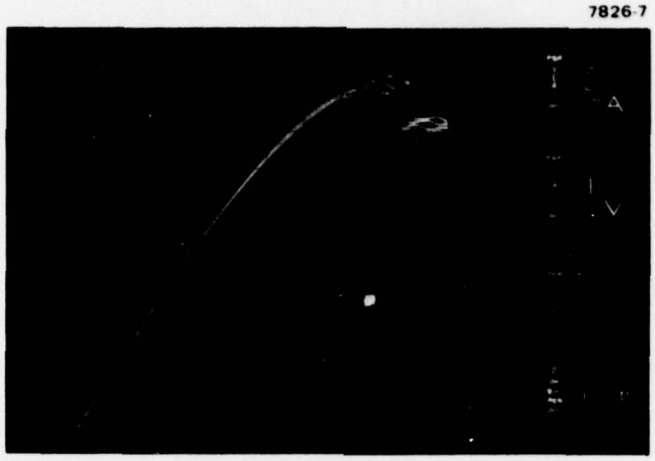
(b) THREE TERMINAL

Figure 37. I-V characteristics of two- and three-terminal TELDs.

Table 5. TELD Threshold Conditions

V_{gc}, V	V_{AC}, V	I_{AC}, mA
0	8.4	18.4
-2	7.9	17.5
-4	7.5	16.5
-6	7.0	15.6
-8	6.5	14.6

6325



(a)

V_{g2} = 0 V, V_{g1} = 0, −2, −4, −6, −8

(b)

V_{g2} = −4, V_{g1} = 0, −2, −4, −6, −8

Figure 38. I-V characteristics of dual-gate TELD.

SECTION 5

CONCLUSIONS

Planar TELDs have been designed, fabricated, and tested. Computer models have been developed for designing and predicting the characteristics of TELDs as a function of device geometry, material parameters, and bias conditions. TELDs have been fabricated on ion-implanted LPE and VPE GaAs. Devices with as high as 24% current drop back in the I-V characteristics have been measured, and frequency dividers which divide the input signal by any integer from two through five have been realized.

Work is continuing on improving the ion-implantation processing with the aim of increasing the depth so that the Nd product will be large enough. E-beam lithography is being used to write 1-μm gates on the 2-μm-high mesas. This involves developing compatibility in the processing steps between photolithography and E-beam lithography. Devices with anodic oxide grown under the pick-off gate are being processed to determine the effect of the interface states and the oxide thickness. Finally, models are being improved to correlate with the measured devices.

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